VECTOR

MICROPOLIS DISK CONTROLLER BOARD

Technical Information Manual

MICROPOLIS 5 1/4" FLOPPY DISK CONTROLLER BOARD

TECHNICAL INFORMATION MANUAL

REVISION A

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Rev. A 11/21/80

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FOREWORD

Audience	This manual is intended for dealers, user's, and service personnel with a moderate knowledge of microcomputers
Scope	It describes what the Micropolis 5 1/4" Floppy Disk Controller Board does, how to test and adjust the board, and how to troubleshoot the board.
Organization	Each section is written at a uniform level of technical depth. "User's Information Sheet" tells the user how to convert to a 56K system and how to change base addresses. "Perspective" tells what the board does by describing the major functional units of the board. "Test and Adjustments" explains how to test and adjust the board and "Troubleshooting" describes how to troubleshoot the board.

TABLE OF CONTENTS

USER'S INFORMATION SHEET

NOTE:

To convert a Micropolis 5 1/4" Disk Controller board from a 48K to a 56K system, remove jumper W1, jumper W4 remains in place.

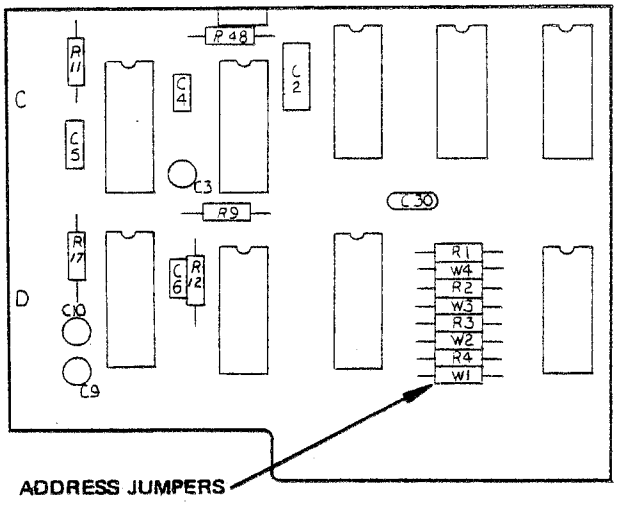
Changing The Controller Base Address

If the controller base address requires changing, the controller may be jumpered at any 1K boundary from C000H to FC00H by performing the following procedure.

a. Referring to illustration below, locate the address jumpers W1 thru W4.

b. Referring to the following table, determine the jumpers required for the desired base address. Install the required jumpers using a short length of insulated wire.

c. Solder in the new jumper(s) using a 25-30 watt soldering iron and resin core solder.



CONTROLLER BASE ADDRESS JUMPER CONFIGURATIONS

	Base Address		ADDRESS BIT / JUMPER A15 N/A	A14 N/A	A13 W1	A12 W2	A11 W3	A10 W4	A9 N/A	A8 N/A	Jumper Installed W1	W2	W3	W4
Standard Address	CO	00 - C3FF	1	1	0	0	0	0	0	0	Y	Y	Y	Y
	C4	00 - C7FF	1	1	0	0	0	1	0	0	Y	Y	Y	N
	C8	00 - CBFF	1	1	0	0	1	0	0	0	Y	Y	N	Y
	CC	00 - CFFF	1	1	0	0	1	1	0	0	Y	Y	N	N
	D0	00 - D3FF	1	1	0	1	0	0	0	0	Y	N	Y	Y
	D4	00 - D7FF	1	1	0	1	0	1	0	0	Y	N	Y	N
	D8	00 - DBFF	1	1	0	1	1	0	0	0	Y	N	N	Y
	DC	00 - DFFF	1	1	0	1	1	1	0	0	Y	N	N	N
	E0	00 - E3FF	1	1	1	0	0	0	0	0	N	Y	Y	Y
	E4	00 - E7FF	1	1	1	0	0	1	0	0	N	Y	Y	N
	E8	00 - EBFF	1	1	1	0	1	0	0	0	N	Y	N	Y
	EC	00 - EFFF	1	1	1	0	1	1	0	0	N	Y	N	N
	F0	00 - F3FF	1	1	1	1	0	0	0	0	N	N	Y	Y
	F4	00 - F7FF	1	1	1	1	0	1	0	0	N	N	Y	N
	F8	00 - FBFF	1	1	1	1	1	0	0	0	N	N	N	Y
	FC	00 - FFFF	1	1	1	1	1	1	0	0	N	N	N	N

Example: To use base address E400, install jumpers at W2 and W3.

I. PERSPECTIVE

1.1 Functional Description

The Micropolis Disk Controller Board (Figure 1-1) is implemented on a 5-by-10 inch PCBA that plugs into the S-100 bus. The controller contains the following major functional units:

a) Control logic to interpret CPU selection and respond to CPU commands.

b) A sector separator that separates sector and index pulses and keeps track of each sector as it passes under the read/write head.

c) Write logic that converts parallel-form bytes from the CPU to serial data suitable for recording on the disk.

d) Read logic that converts the serial data from the disk to parallel-form bytes for transfer to the CPU.

e) Bootstrap PROMs for reading sector zero of the system disk into RAM, then starting the program in RAM.

1.1.1 Disk Data Format

Data is recorded on the disk in concentric tracks. The outermost track is track zero. Each track is divided into 16 sectors. The beginning of each sector is indicated by a sector hole punched in the disk. An index hole is located halfway between the holes for sector 15 and sector zero. The sector and the index hole are sensed by a photo transistor in the disk drive. Each disk sector consists of a preamble, sync byte, header, data, a checksum, and a postamble. Each of these fields are described below.

Preamble

The preamble is composed of approximately 40 bytes of zero (0) data bits.

The preamble is automatically generated by the disk controller and is necessary to provide tolerance for the mechanical alignment and electrical characteristics of the sector/index sensor. It also provides a field of known data pattern for synchronization of the read data decoder.

Sync Byte

The sync byte is a byte of data (FFH) which is used in the disk controller to define the beginning of useful data.

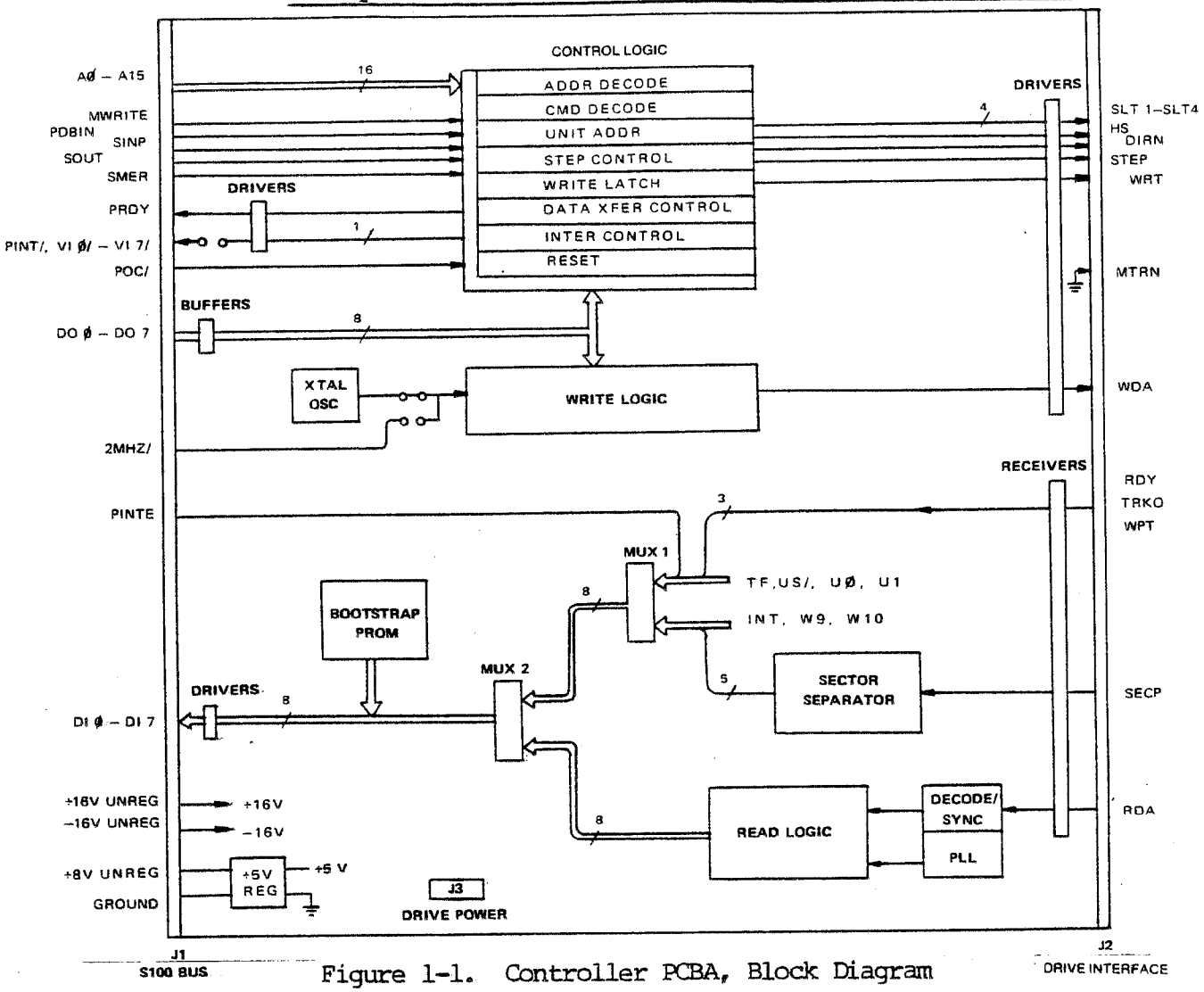


Figure 1-1. Controller PCBA, Block Diagram

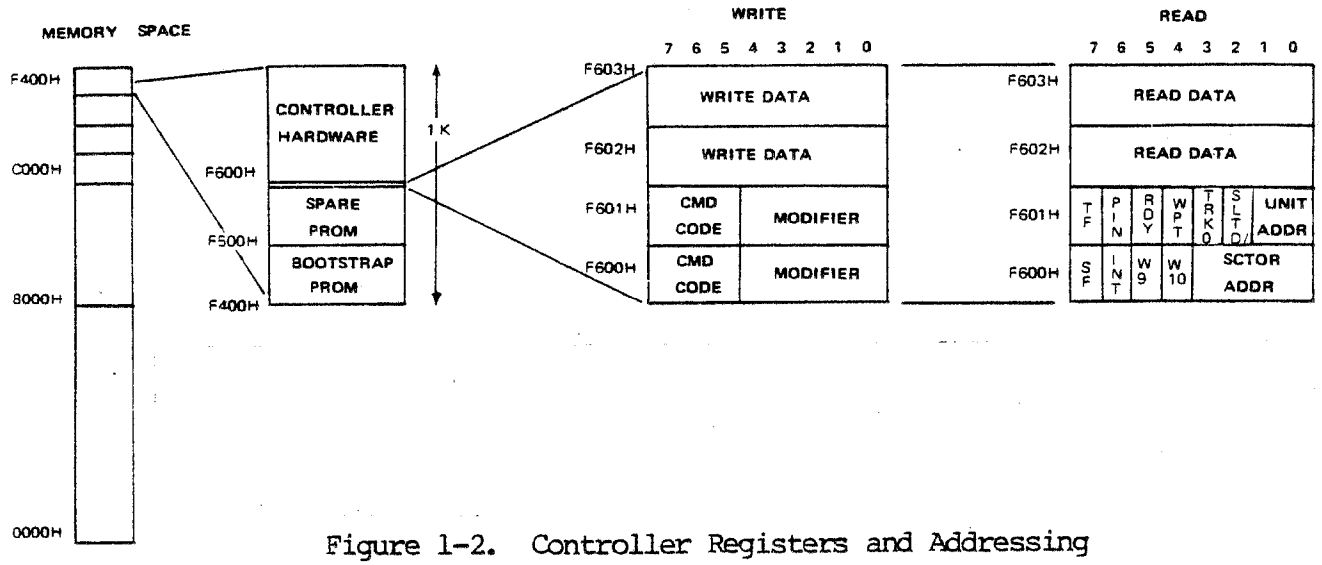


Figure 1-2. Controller Registers and Addressing

Header

The header is a 2-byte block consisting of the binary track address of the track on which the sector resides (0-76 (34)) and the address of the sector (0-15). The header is used to verify that the proper sector is being accessed in a disk I/O operation.

Data

The data field consists of 266 bytes of user data.

Checksum

The checksum is a one byte error detection code that provides error detection in read operations. The checksum is computed by the CPU as follows:

a) The accumulator and carry are initially cleared;

b) Each byte of the header and data fields is added to the accumulator with carry.

In write operations, the computed checksum is written immediately following the data field. In read operations, the checksum is recomputed from the read data and is compared with the checksum byte which is read. If they do not compare, a read error has occurred.

Postamble

The rest of the sector from the checksum to the next sector hole is filled with zero data bits. The length of the postamble allows for the mechanical tolerance in the placement of sector holes on the disk and tolerance for disk speed and write clock variations.

1.1.2 Controller Registers

The controller is accessed using the memory-mapped I/O technique; that is, the controller command, status, and data registers are treated as memory addresses, so that the controller read/write commands are actually memory reference instructions. See figure 1-2 for a pictorial illustration of the controller registers and the standard address configuration.

One kilobyte of the CPU's memory space is allocated for use by the controller. The upper 512 bytes are reserved for operating the controller and the lower 512 bytes are allocated for the bootstrap PROMs. Because only half of the available PROM is used, only half of the lower space is used. The controller hardware registers occupy the the first four locations of the upper 512 bytes; and the remainder of the address space duplicates these four addresses over and over.

Jumpers W1 through W4 allow the controller to be located at any one of

the upper 16 1K blocks of CPU memory space (base addresses C000H to FC00H). The controller is normally configured with only jumper W4 installed, selecting the memory block starting at F800H, as shown in figure 1-2. The controller command, status, and data registers are also indicated in this figure and are accessed by the appropriate CPU memory read and write commands.

Command register

The command register, located at FA00H or FA01H for CPU memory write operations, provides for drive unit/head selection, interrupt control, write enable, track-to-track stepping, and controller reset. The CPU sets the command code in bits 7, 6, 5 and sets the modifier bits in 0 thru 4. Bit specifications for the command register are shown below.

Command Code (bits 7,6,5)	Command	Modifier (bits 0-4)
0		
1	Select Drive/Head	(Bits 0,1: Select drive unit address (0-3) (Bit 4: Select head: 0=lower; 1=upper
2	Interrupt Control	(Bit 0: =0 Disable sector interrupt =1 Enable sector interrupt
3	Step 1 track	(Bit 0: =0 Step out (decrease track number =1 Step in (increase track number
4	Set WRITE	Not used
5	Reset Controller	Not used
6	Not used	Not used
7	Not used	Not used

Sector Register

The sector register, located at FA00H for CPU memory read operations, contains the address of the sector currently passing under the read/write head, and contains the sector flag and sector interrupt flag as they occur. The sector register forms controller status byte zero. Bit specifications for the sector register are shown below.

Bits	Definition
0-3	Sector Address: Address of the sector passing under the read/write head of the select drive.
4	Reserved: Jumper W10
5	Host CPU Speed: Jumper W9 is installed according to host CPU speed as follows: 1 = 2MHz CPU (W9 not installed) 0 = 4MHz CPU (W9 installed)
6	Sector Interrupt Flag: Indicates an interrupt request has been generated by a sector pulse. Flag is reset by issuing a reset or an interrupt disable command. (Not used by Micropolis software).
7	Sector Flag: Indicates the sector address is valid and that a read or write operation may be performed. Flag is true for 30 usec at the start of each sector. All data transfers must be intiated within 100 usec of the flag going true.

Status Register

The status register, located at FA01H for CPU memory read operations contains drive select and status bits, CPU interrupt status, and a flag which enables the CPU to synchronize disk read and write operations. The status register forms controller status byte one. Bit specifications for the status register are shown below.

Bits	Definition
0-1	Unit Address: Address of the currently selected drive. Address is valid only if SLTD/ is true (0).
2	SLTD/:Unit selected . This flag is low true, ie., 0=A drive is selected. 1=No drive is selected. SLDT/is true if a drive has been selected and the 4-second timer has not expired. SLTD/is low true so that the software may detect when the controller is not installed (non-existant memory references yield 0FFH).
3	TK0: Track 0 status from selected drive.
4	WPT: Write protected status from selected drive.
5	RDY: Ready status from the selected drive. When true, indicates the drive is ready to perform commands.
6	PINTE:PINTE status from the S-100 BUSS.
7	TF:Transfer flag. In write operations, indicates that the controller is ready to accept data from the computer. In read operations, indicates that the controller has data available to the computer. When the software detects the transfer flag has set, all data transfers are performed by accessing the controller data register, which automatically synchronizes the transfer by use of the PRDY line.

Write Data Register

The write data register, located at FA02H/FA03H for a CPU memory write operation, enables the CPU to write data on the disk. If the write data register is referenced when the transfer flag is set during a write operation, the controller expects a data byte to be on the S-100 bus data lines. The PRDY line will be set true for 1 bit time (4 usec). (See the status register description for the definition of the transfer flag).

Read Data register

The read data register, located at FA02/FA03H for a CPU memory read operation, enables the CPU to read disk data after it has been assembled into parallel form by the controller. If the read data register is accessed when the transfer flag is set during a read operation, the controller will hold the PRDY line false until a byte of data is available. The controller will then place the data on the S-100 bus lines and set the PRDY true for 1 bit time (4 usec). The data will only be available for this 1 bit time period.

1.1.3 S-100 Bus Signals definition

Pin assignments and identification of S-100 bus signals used by the controller are shown below. Bus timing for handshaking and data transfer are shown in figure 1-3.

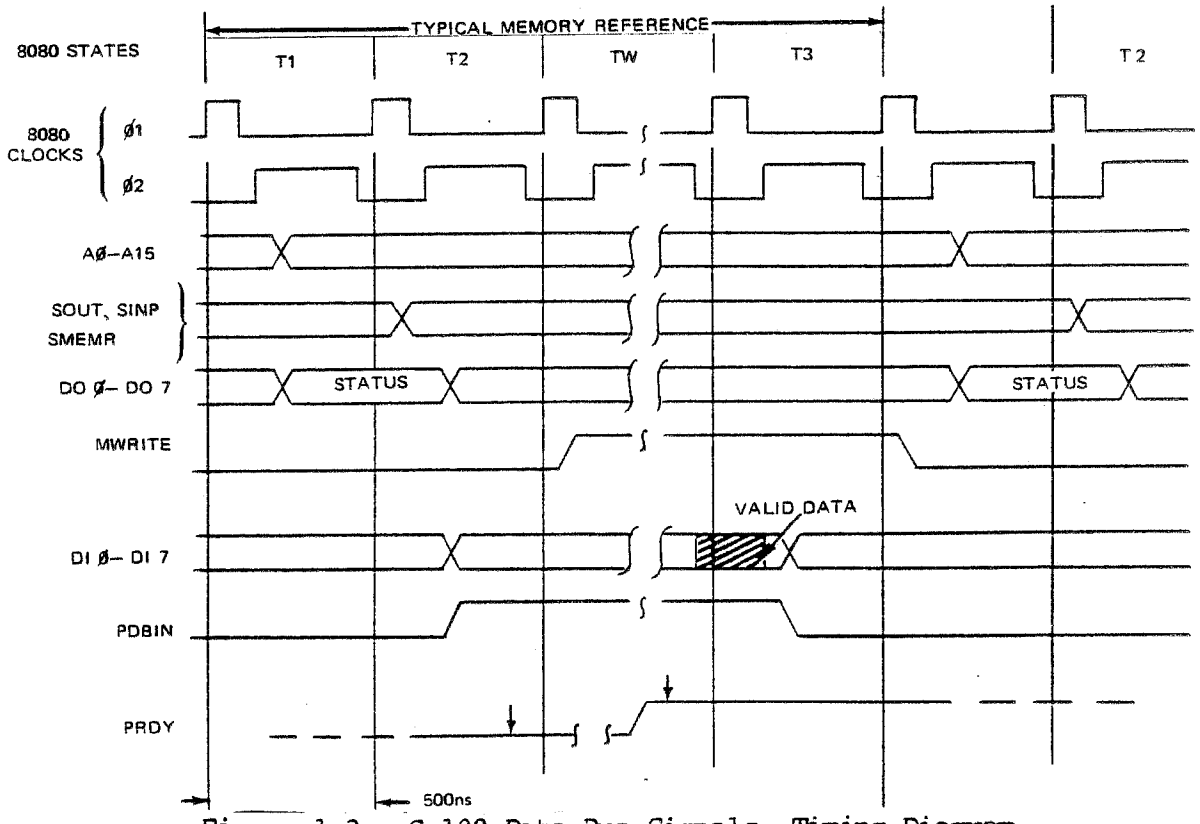


Figure 1-3. S-100 Data Bus Signals, Timing Diagram

DISK CONTROLLER S-100 BUS INTERFACE

Signal	Pin	Dirn	Description	Signal	Pin	Dirn	Description	Note
A00	79			SINP	46	IN	I/O Input Cycle	
A01	80			SOUT	45	IN	I/O Output Cycle	
A02	81			SMEMR	47	IN	MEM Read Cycle	
A03	31			MWRITE	68	IN	MEM Write Strobe	
A04	30			PDBIN	78	IN	CPU Data In Strobe	
A05	29			PRDY	72	OUT	CPU Ready Line	
A06	82			POC/	99	IN	Poweron Clear	
A07	83	IN	Address					
A08	84		Bus	2MHZ/	49	IN	2.0 MHz Xtal Clock	4
A09	34							
A10	37			PINTE	28	IN	CPU INTE Line	5
A11	87			PINT/	73	OUT	CPU INT Line	5
A12	33							
A13	85			V10/	4			5
A14	86			V11/	5			5
A15	32			V12/	6			5
				V13/	7	OUT	Vectored Interrupt	5
D00	36			V14/	8		Lines	5
D01	35			V15/	9			5
D02	88			V16/	10			5
D03	89	IN	Data Out	V17/	11			5
D04	38		Bus					
D05	39			GND	50	IN	Ground	
D06	40			GND	100	IN	Ground	
D07	90							
				+8V	1	IN	+8V Unreg	
DI0	95			+8V	51	IN	+8V Unreg	
DI1	94							
DI2	41			+16V	2	IN	+16V Unreg	6
DI3	42	OUT	Data In	−16V	52	IN	−16V Unreg	
DI4	91		Bus					
DI5	92							
DI6	93							
DI7	43							

NOTES:

1. Slash (/) at end of signal name indicates Low True polarity.
2. All signal lines at TTL levels. Input lines require 1.0 mA max drive current. Output lines driven by 74367 (32 mA sink).
3. Signal lines with notes are optional and are not used in the standard Micropolis controller configuration.
4. Jumper option selects 2 MHz bus clock for write circuits instead of internal oscillator.
5. Jumper option generates interrupt on PINT/ or V10/ thru V17/ on occurrence of each sector pulse. PINTE indicates current CPU interrupt status.
6. +16V power for optional disk drive power connector.

1.1.4 Control Logic

The control logic interprets the selection of the controller by the CPU (Address decode), decodes the command byte to determine the selected drive unit and to execute the CPU commands, controls data transfer between the drives and the CPU, and generates CPU interrupt signals corresponding to sector pulses.

Address Decode (See sheet 2 of the schematic)

The address decode consists of decoder D8 and its associated NAND gate and inverters. It monitors the address lines from the CPU to interpret selection of the controller.

Whenever an address is within the 1K block assigned to the controller, D8-9 will go low, and will be inverted by the C7-8 to form BSEL (board select). Also, the low at D8-9 will be gated at D6-10 with the inverse of A9 to form CSEL (controller select). CSEL is inverted by C7-4 to form CSEL/, and also be gated with A1 to form DSEL (data select). When CSEL and MWRITE (memory write) are high and A1 is low, C8-6 goes low to for CMD/ (command code).

Command Decode (See sheet 7 of the schematic)

Commands are decoded by decoder D3 which examines the command modifier bits from the CPU and generates the controller command codes. D3 examines bits from the CPU and generates the controller command codes. D3 examines CMD/ and data bits D5, D6, D7, and generates one of five commands: ADRC/ (address command for selected drive), INTC/ (interrupt command), STEPC/ (step command), WRTC/ (write command, and RSTC/ (reset command).

Unit Address Control (See sheet 8 of the schematic)

The unit address control consists of register B3 and assorted NOR gates and line drivers. It examines data lines from the CPU, stores the selected drive and head addresses, and generates drive and head select signals for the drive interface.

When RST/ (reset) is high and a drive unit select command is executed to form ADRC/, B3 is clocked and stores the contents of D0, D1 (drive address) and D4 (head address). Simultaneoulsy B3-10 is clocked causing US (unit select) to set. B4 decodes U0 and U1 into four drive select signals which are then gated with US by interface drivers B5. US remains set until it is cleared by a low RST/ as the result of a four second timeout or an RSTC/ command. For a double sided drive, B3-15 selects either the lower (0) or the upper (1) head.

Step Control (See sheet 8 of the schematic)

Step control is accomplished by flip-flop B2 and its associated inverter C7-2 and line drivers B6-6 and B6-12. Figure 1-4 shows the circuit timing. When a

step command is issued, STEPC/ goes low for approximately on half microsecond; it is inverted by C7-2 and drives the step line via B6-12. B2-9 is clocked by the rising (leading) edge and copies the state of D0, which will be high for a step in command and low for a step out command. The output of B2-9 drives the DIRN (direction) line via B6-6. Consecutive same-direction step pulses must be separated by 30 milliseconds; opposite-direction pulses by 40 milliseconds for drive operation.

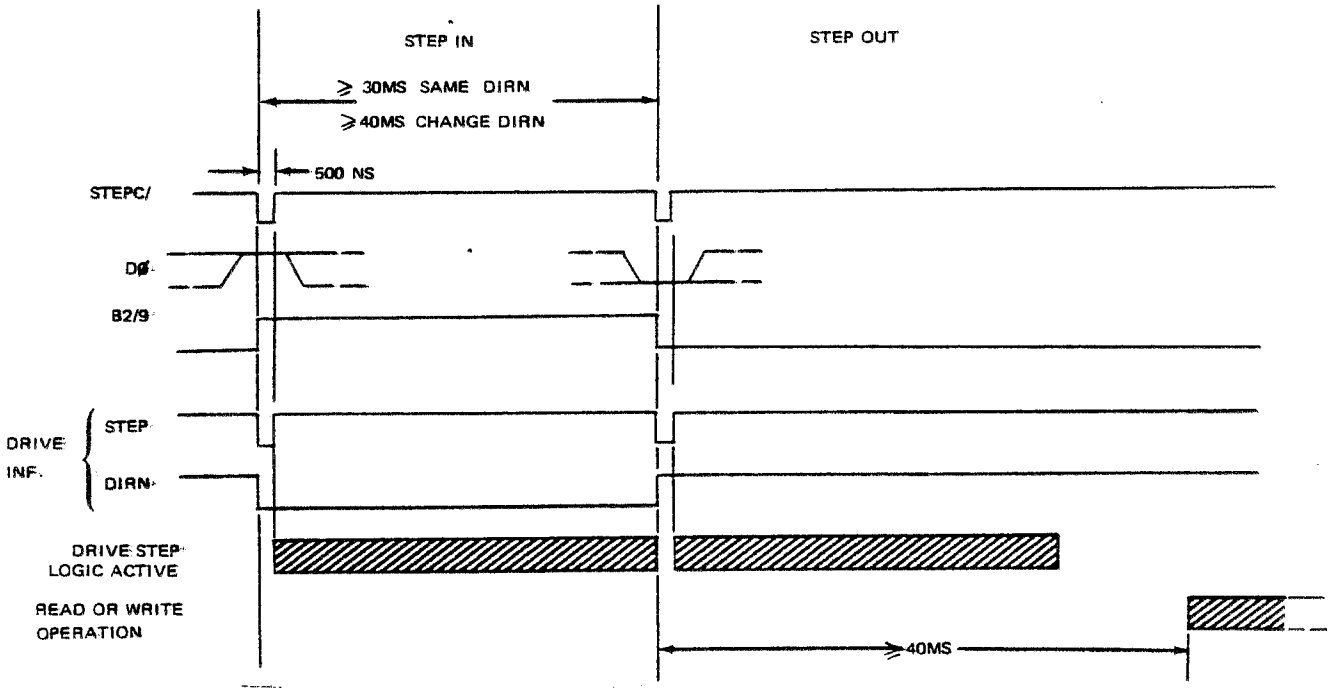


Figure 1-4. Step Control Signals, Timing Diagram

Write Latch

The write latch logic consists of flip-flop B2-5 and its reset logic. When a write command is issued, WRTC/ goes low and the rising (trailing) edge sets flip-flop B2-5. The WRT (write enable) output at B2-5 enables the controller write circuits and asserts the WRT interface line via B6-6 (See sheet 6 of the schematic). Writing occurs in the selected drive when WRT is true. B2-5 is normally reset by SP/ (sector pulse) going low at the end of the sector; it will also be reset if RST/ is low or RDY (ready drive) is not present.

Reset Circuits (See sheet 7 of the schematic)

The reset circuit generates RST/, the general reset signal for the controller. The circuit consists of a four-second one-shot D1-5 and associated logic.

D1-5 is a retriggerable one-shot which is triggered by DIG/ each time the CPU reads from the controller status or data registers. This occurs many times a second when the controller is in use causing D1-5 to remain high. If there is no disk activity for a period of four seconds, D1-5 goes low causing a low RST/. Other inputs to RST/ are RSTC/ (reset command) and POC (S-100 power-on clear).

Data Transfer Control (See sheet 6 of the schematic)

This logic generates three signals associated with the control and synchronization of data transfers between the controller and CPU. Waveforms are shown in figure 1-5.

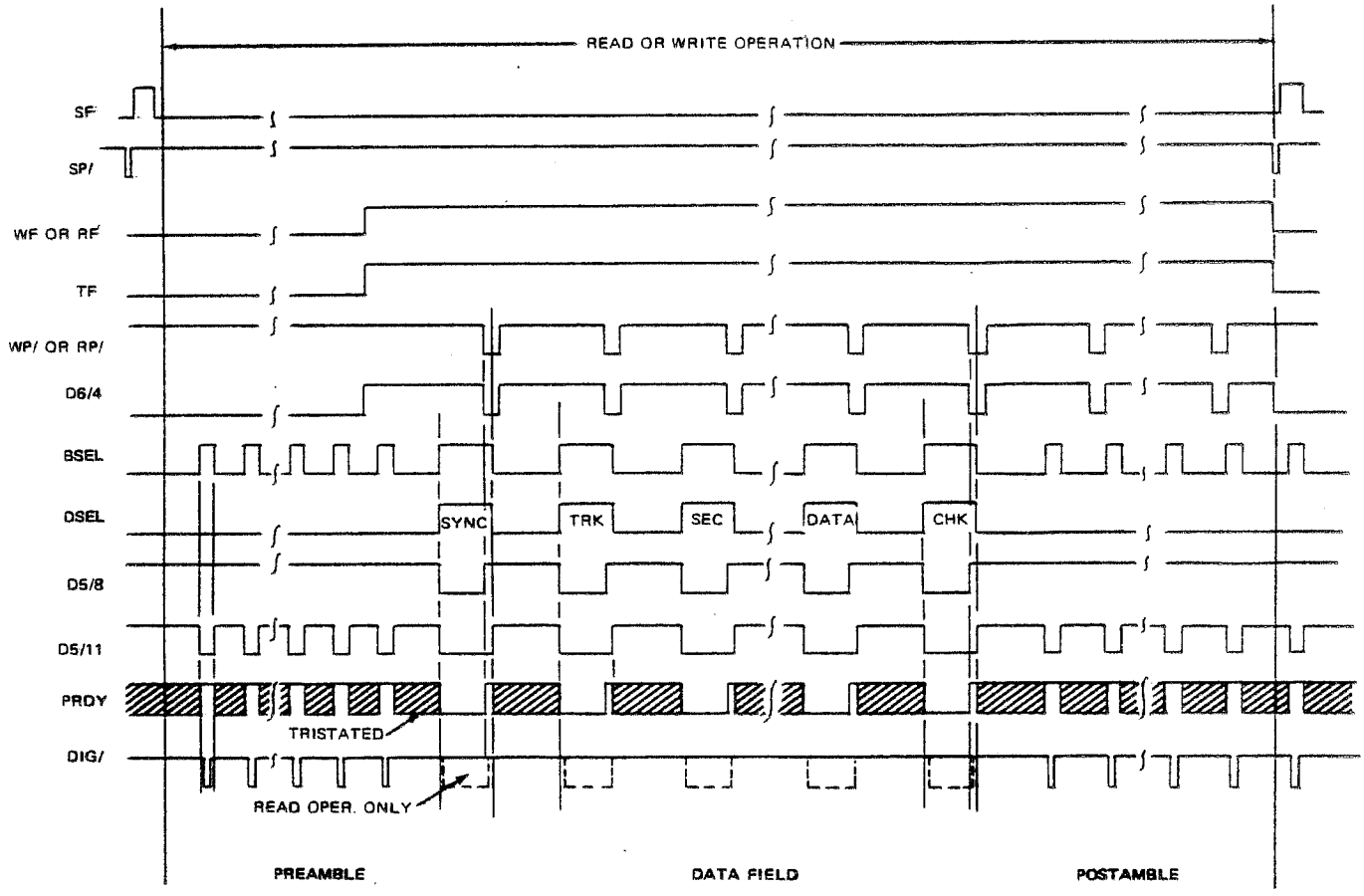


Figure 1-5. Data Transfer Control Signals, Timing Diagram

TF: Transfer Flag

This flag goes true one byte-time before the first (sync) byte is to be transferred to/from the controller. It is formed by gates D6-1 and D6-13 by or'ing together WF (write flag) from the write logic and RF (read flag) from the read logic. TF is sensed by the CPU by reading status byte 1.

PRDY: Processor Ready

This line connects to the CPU ready input. When PRDY is low, the CPU executes continues WAIT states, freezing program execution in the middle of the current machine cycle. The address data out lines remain valid during this time. This facility is used to synchronize the transfer of disk read or write data between the CPU and controller.

The tri-state PRDY gate (D9-13) is enabled by NAND D8-11, and when enabled, gates the output of D5-8 onto the PRDY line. PRDY is enabled when the controller is being accessed (BSEL high) during a memory reference instruction (SINP and SOUT both low).

D5-8 is normally high except when the read or write data register is being accessed (DSEL high), TF is high (data area of the sector), and WP/ and RP/ are both high (controller not ready to accept a byte of write data, or has not assembled a complete byte of read data). When the controller is ready for the transfer, WP/ or RP/ goes low for one-bit time allowing the software loop to proceed.

DIG/: Data In Gate

This signal gates controller status, read data, or PROM information onto the S-100 bus data in lines D10 thru D17 (See sheet 5 of the schematic). DIG/ (C8-8) goes low when the controller is addressed (BSEL high) during memory read instructions (SMEMR and PDBIN both high).

Interrupt Control (See sheet 7 of the schematic)

When enabled, the interrupt control logic generates an interrupt as the sector flag (SF) goes high at each sector boundary. Figure 1-6 illustrates the timing of this circuit. The interrupt may be jumpered to PINT/ (processor interrupt) or one of the vectored interrupt lines VI0/ thru VI7/. The logic consists of interrupt enable flip-flop D2-5, interrupt flip-flop D2-9, and the driver D10-13.

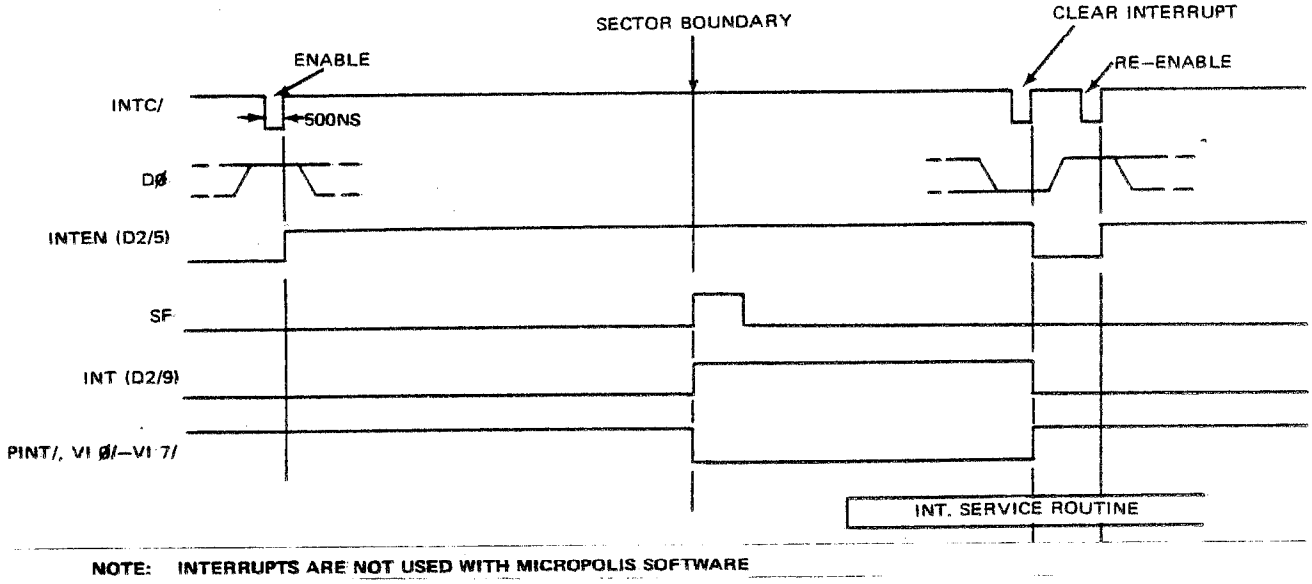


Figure 1-6. Interrupt Signals, Timing Diagram

When an interrupt control command is issued, D2-5 is either set or reset depending on the state of the modifier bit D0. When set, interrupts are enabled allowing D2-9 (INT) to set at the following sector boundary (rising edge of SF). The resulting low at D10-13 drives the desired S-100 interrupt line by means of a jumper connection. The interrupt is cleared by the interrupt service routine by issuing another interrupt control command with D0=0.

The interrupt logic is initially cleared by RST/ low.

1.1.5 Sector Separator (See sheet 6 of the schematic)

The sector separator uses SECP (the drive sector hole photosense output received at B7-4) to generate the sector timing signals ROS (read one-shot) and its compliment ROS/, WOS/ (write one-shot), SF (sector flag), SP/ (sector pulse), and S0 thru S3 (sector count signals). It consists of one-shots C2, C1, and D13, and four-bit counter C3. Figure 1-7 illustrates the timing of this circuit.

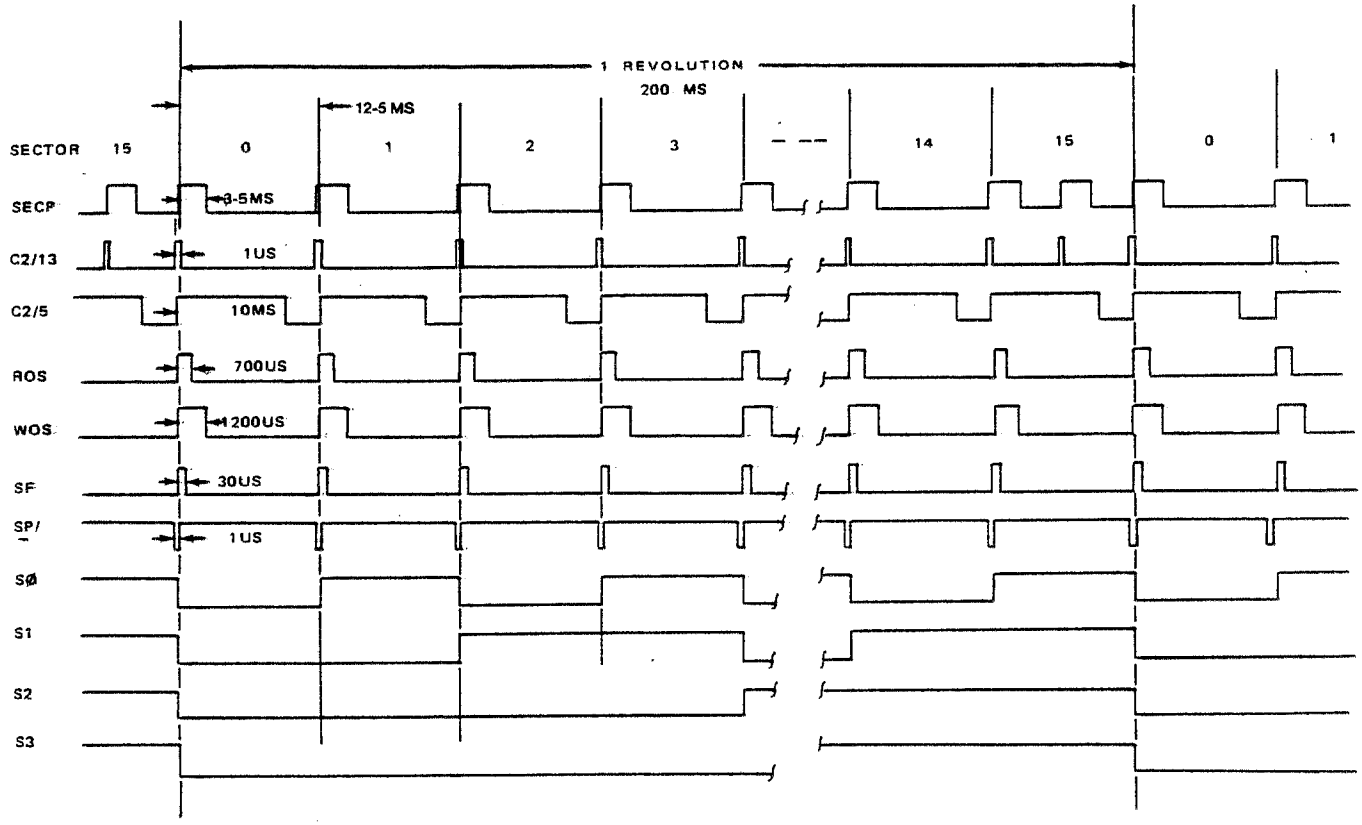


Figure 1-7. Sector Separator Signals, Timing Diagram

ROS is generated as follows: one-shot C2-13 shapes the leading edge of SECP into a one-microsecond pulse which is used by one-shot C2-5 to form a pulse of approximately three quarters of a second period; the pulse bridges the time during which the index pulse occurs. The pulse at C2-5 triggers one-shot C1-13, which forms a 700 microsecond ROS period to provide time for PLL and read logic-decode circuits to synchronize before a sector is read. C2-5 also triggers one-shot C1-5 which generates a 1200 us time period during which the preamble is written for write commands.

SF is a 30-microsecond pulse formed when one-shot D1-13 is triggered by the leading edge of the C2-5 pulse; The high formed at D1-13 is delayed through AND gate C6-3 by RC network C7 and R13 to form SF. This delay (approximately 200 ns) ensures that the sector counter is stable at the new sector address when the CPU senses SF true.

SP/ consists of a one-microsecond low true pulse for each of the 16 sector holes in the diskette. Each pulse defines the end of one sector and the beginning of the next. No pulse is generated for the index hole. It is formed by gating C2-13 with C2-12.

S0 thru S3 are the outputs of a 4-bit counter C3, which is incremented at each sector boundary. These lines indicate the binary address (0-15) of the sector currently under the read/write head. The counter is synchronized with index by loading a count of 15 when the index hole is sensed. SF and S0 thru S3 are sampled simultaneously by the CPU by reading status byte 0.

1.1.6 Write Circuits (See sheet 3 of the schematic)

The write circuits accept parallel data bytes DO0 thru DO7 from the CPU via D9 and D10. The data is serialized then decoded into MFM form to generate WDA (write data). This signal is routed to the select drive via B6-10 (See sheet 8 of the schematic). This logic consists of the write bit and byte counters, shift register, encoding the pulse shaping circuits.

Write timing is derived from a 2 MHz OSC (oscillator) signal from a crystal oscillator (See sheet 7 of the schematic). An alternate 2 MHz signal may be obtained from the S-100 data bus via J1-49 if jumper W12 is installed.

The write logic is normally configured for MFM encoding: Double frequency encoding can be used in place of MFM if jumpers W6 and W7 are removed and jumpers W5 and W8 are installed. The Micropolis software is configured for MFM operation only. Figures 1-8 and 1-9 provide timing information on ther write circuits. Write timing is derived from a 2 MHz OSC/ (oscillator) signal from a crystal oscillator (See sheet 7 of the schematic). An alternate 2 MHz signal may be obtained from the S-100 data bus via J1-49 if jumper W12 is installed and W11 is omitted.

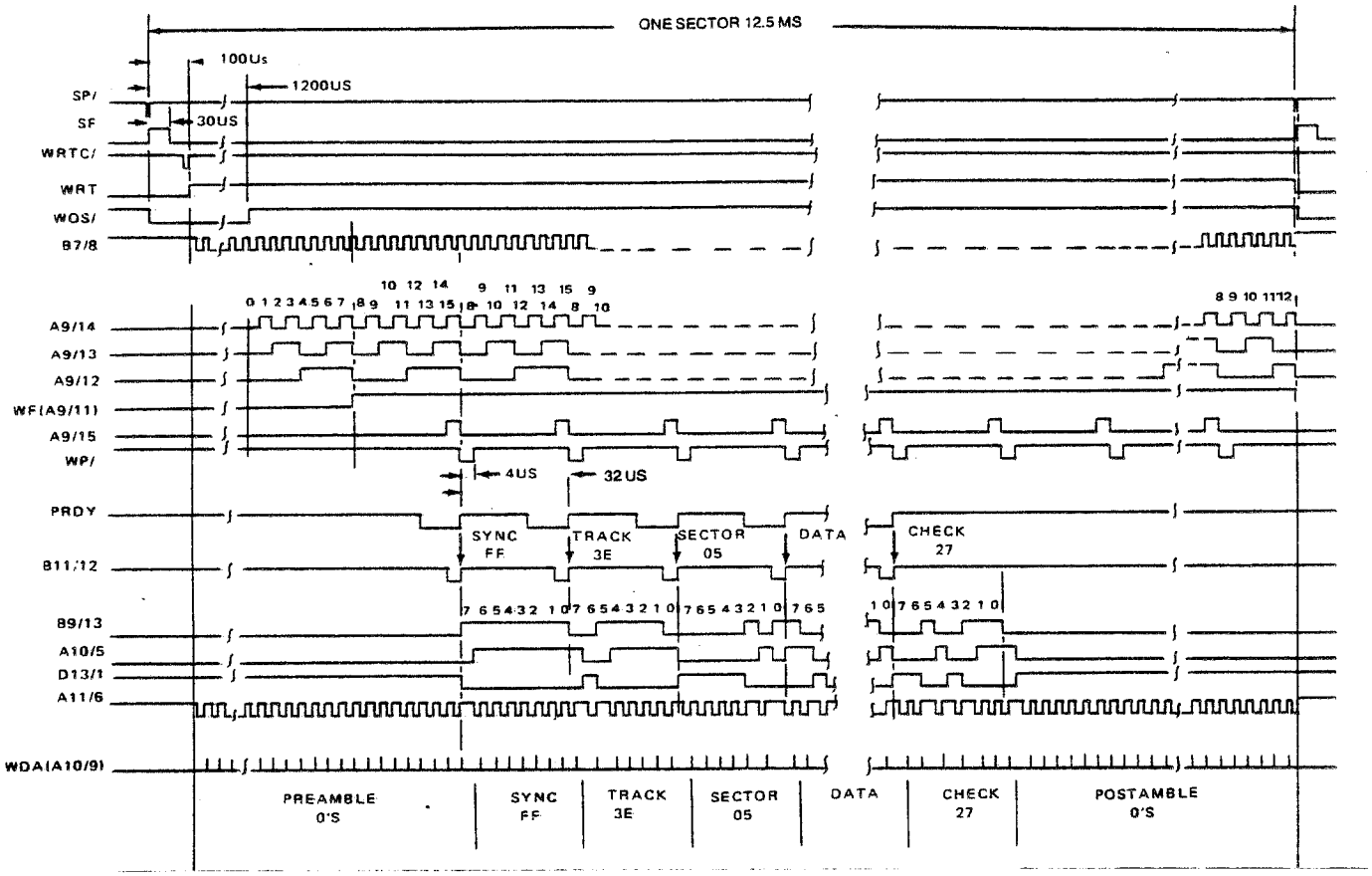


Figure 1-8. Write Logic (MFM), Timing Diagram

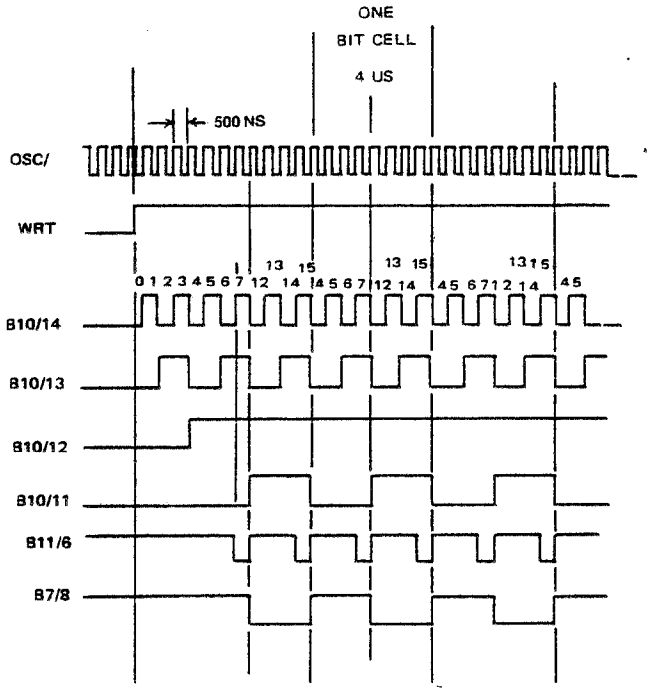


Figure 1-9. Write Clocking Logic, Timing Diagram

The following sequence of events occurs when a sector is written onto the diskette:

a. The disk I/O driver software selects the required drive and moves the positioner to the desired track using DRIVE SELECT and STEP commands to the controller.

b. The driver continually reads status byte 0 looking for SF true with the desired sector address.

c. When the desired sector is found, a SET WRITE command must be issued within 70 us (i.e., within 100 us of the physical beginning of the sector). This sets the WRT flip-flop in the controller causing the preamble to be written onto the diskette.

d. The driver continually reads status byte 1 looking for the TF (transfer flag) true. This occurs at the end of the preamble when the sync byte is about to be written.

e. The driver must write the sync byte pattern (FFH) to the write data register within 20 us after detecting TF true. The controller responds by pulling the PRDY line low thus holding the sync pattern on the DATA OUT lines until it is ready to accept the byte.

f. One-byte time (32 us) after TF goes true, the controller copies the synch byte into the write register and raises the PRDY line allowing execution of the software loop to proceed.

g. During the following byte-time, the sync byte is serialized, encoded, and written onto the disk. At the same time, the driver accesses the following byte (cylinder address), computes a partial sumcheck, and writes the byte to the write data register causing PRDY to go low again.

h. Steps f and g are repeated for each byte of the header and data fields. The sumcheck byte is then written immediately after the last data byte.

i. The controller automatically fills the remainder of the sector with an all-zeroes pattern. When the following sector pulse is encountered, WRT is automatically reset in the controller ending the write operation.

Write Bit Counter (See sheet 3 of the schematic)

The write bit counter consists of counter B10 and NAND gates B7-8 and B11-6.

The WRT signal from the write latch enables bit counter B10 and the remainder of the write circuits. B10 then counts the 2 MHz OSC/ pulses and produces the waveforms shown in figure 1-9. Output B10-11 (OSC divided by eight) consists of a square wave with a period of one bit-time (4 us). This is inverted by B7-8 and used to clock the byte counter A9, and data shift register B9. NAND gate B11-6 decodes a count of 7 or 15 in B10 causing a count of 12 or 4 to be loaded into the counter.

Byte Counter (See sheet 3 of the schematic)

The byte counter consists of A9, flip-flop B12-5, and inverter D14-4. The byte counter counts off consecutive groups of 8 bits which correspond to each byte of data recorded on the diskette. The signal WP/ (write pulse) goes low for one bit-time at the beginning of each byte.

Counter A9 is inhibited by WOS/ low while the preamble is being written (See figure 1-7). After approximately 1200 us, WOS/ goes high allowing A9 to be clocked by the rising edge of each bit-time pulse from B7-8. A9 counts off consecutive bits of data until it reaches the count of eight; at that time, WF (write flag) goes high indicating that the sync byte is about to be written. A9 then continues counting until 15 is reached, at which time A9-15 (carry output) goes high causing A9 to load a count of eight, and then to continue in the sequence 8-15, 8-15, etc. Each 15 count (A9-15 high) corresponds to the last bit of a byte. This signal is delayed by B12-5 to form WP/ which goes low during the following bit-time. WP/ low causes PRDY to go high for 4 us, allowing the software loop to proceed.

Shift Register (See sheet 3 of the schematic)

The shift register logic consists of a parallel-to-serial register B9 and NAND gate B11-12. The shift register converts the parallel DO0 thru DO7 data inputs to serial data output at pin 13, as shown in figure 1-8.

During the last bit of each byte, A9-15 high causes B11-12 to go low provided that the CPU is writing to the write register address (DSEL and MWRITE both high). This places the shift register in load mode causing the contents of DO0 thru DO7 to be copied into the register on the following clock. This information is shifted right and appears at B9-13 in serial form during the following byte-time.

After the sumcheck has been written, the software makes no further reference to the write register and the register is not loaded. A continuous stream of zeroes entering at B9-1 is shifted through the register to form the postamble pattern.

Encoding and Pulse Shaping Circuits (See sheet 3 of the schematic)

The encoding circuit consists of A10-5, D13-1, and A11-6. The pulse shaping circuit consists of D13-4 and A10-9. These circuits encode and shape the data stream from B9-13 to form WDA.

The rules for MFM (double density) and DF (single density) encoding are usually stated as follows:

Rule 1 MFM and DF: A flux transition is written in the middle of a cell if the current data bit is 1.

Rule 2 MFM: A flux transition is recorded at the beginning of a cell if the current and preceeding data bits are both 0.

DF: A flux transition is recorded at the beginning of every cell.

In this implementation of the logic, rule 2 has modified to an equivalent form as follows:

Rule 2A MFM: A flux transition is recorded at the end of a cell if the current and subsequent data bits are both 0.

DF: A flux transition is recorded at the end of every cell.

Serial data from B9-13 is first delayed one bit-time by A10-5. This flip-flop contains the data bit currently being encoded. D13-1 and A11-6 then perform the encoding function as described above, where gate inputs A11-4/5 introduce the data transitions (Rule 2A). Output A11-6 goes low for half a bit-time for each transition to be recorded.

D13-4 and A10-9 shape this signal to form WDA which consists of a 0.5 us high-true pulse for each transition. Line driver B6-10 transmits WDA to the selected drive.

1.1.7 Read Circuits (See sheets 4 and 9 of the schematic)

The following sequence of events take place when a sector is read from the disk:

a. The disk I/O driver software selects the required drive and moves the positioner to the desired track using DRIVE SELECT and STEP commands to the controller.

b. The driver continually reads status byte 0 looking for SF true with the desired sector address.

c. When the desired sector is found, the driver continually reads status byte 1 looking for TF (transfer flag) true. This occurs one byte-time before the first (sync) byte of the sector is available to transfer to the CPU. Note that no explicit SET READ command is required since the controller is always attempting to read when it is not writing.

d. The driver must attempt to read this byte from the read data register within 20 us after detecting TF true. The controller responds by pulling PRDY low until the byte is fully assembled.

e. When the byte is assembled, PRDY goes high for one bit-time allowing the transfer to be completed. The driver must now process the sync byte and attempt to access the following byte (cylinder address) in less than one byte-time. This causes PRDY to go low again.

f. Step e is repeated for each byte of the header, data, and sumcheck fields.

The driver recomputes the sumcheck from the header and data fields and compares this against the sumcheck read from the disk. A discrepancy indicates a disk data transfer error.

The read electronics consists of phase-locked loop circuit (PLL), data decoder, clock synchronization circuit, serial-to-parallel converter, and control logic.

PLL (See sheet 9 of the schematic)

The purpose of the PLL is to provide a clock signal for decoding purposes which maintains a fixed phase relationship with the incoming read data signal, RDA. The PLL is a feedback system consisting of a phase comparator, a low-pass filter, error amplifier, and a voltage controller oscillator (VCO).

A block diagram is shown in figure 1-10 with no input signal applied, the error voltage is zero and the VCO oscillates at its center frequency fo. When an input signal is applied, the phase comparator compares the phase and frequency of the input with the VCO output, and generates an error voltage Ve(t) that is related to the difference of the two signals. This error voltage is filtered, amplified, and routed to the control input of the VCO. Thus the control voltage Vd(t) forces the VCO frequency to vary in a direction that reduces the frequency difference between fo and the input signal. If the input signal fs is sufficiently close to fo, the feedback nature of the PLL causes the VCO to lock with the incoming signal. When locked, the VCO frequency is identical to the input signal, except for a small phase difference which is necessary to generate the correction signal which maintains the VCO at the input data frequency fs. In this way, the PLL can track variations in the disk speed, generating a continuous clock having a fixed phase relationship with the incoming data, and which can be used to decode the data pattern.

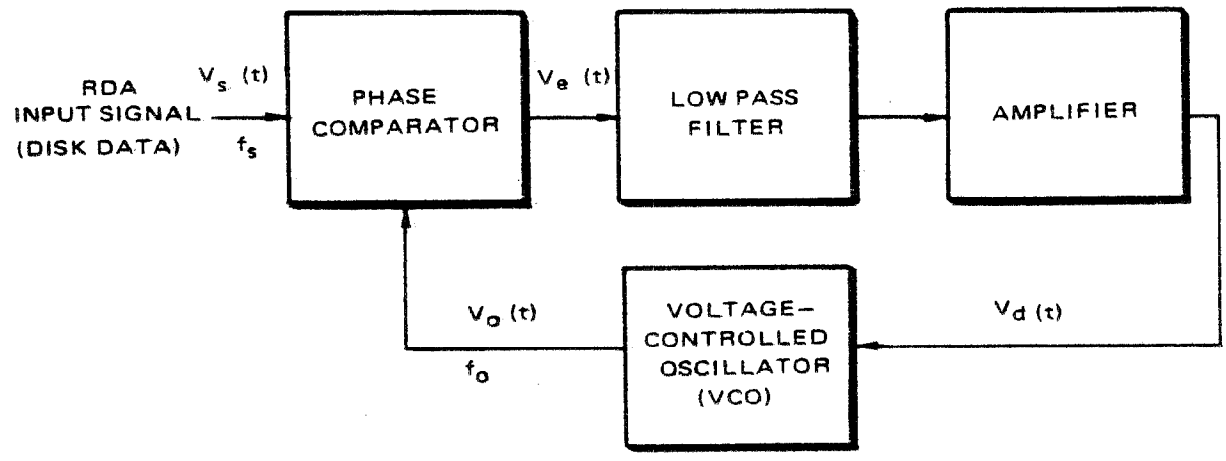


Figure 1-10. Phase Locked Loop (PLL), Block Diagram

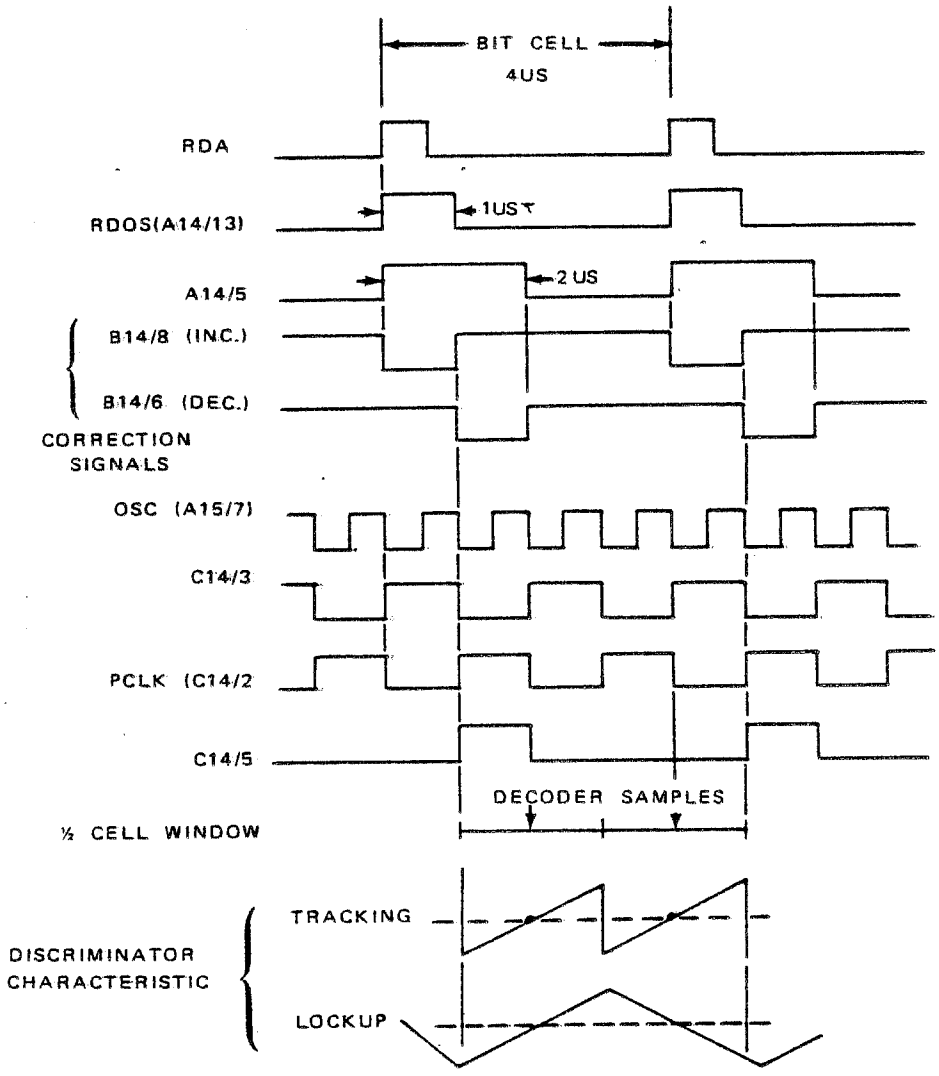


Figure 1-11. PLL Circuits (MFM), Timing Diagram

Figure 1-11 illustrates the timing of the PLL circuits. RDA is received at B7-10 (See sheet 8 of the schematic) and applied to one-shot A14-5 to produce a 2 us pulse for each flux transition read from the disk. The one-shot output connects to a phase comparator consisting of flip-flop C14-5 and NAND gates B14-11, -8, and -6. The VCO oscillates at four times the data rate, and its output A15-7 is first divided by two by C14-3 before clocking the comparator flip-flop C14-5. Jumper W14 and W16 are installed for MFM operation or W13 and W15 are installed for DF operation. The PLL timing diagram for MFM is shown in figure 1-11.

Correction signals generated by B14-8 and B14-6 are applied to a balanced low pass filter formed by R30, R32, and C17 on one leg and R31, R33, and C18 on the other leg. The filter output is amplified by differential amplifier B15, which in turn drives the control input to the VCO. The center frequency is adjusted by potentiometer R40, and should be set at 1.0 MHz for MFM (0.5 MHz for DF with no data input).

Another one-shot A14-5 (RDOS), delays the leading edge of each RDA pulse by 1.0 us before input to the read decoding logic (See sheet 4 of the schematic). When the PLL is locked, the falling edge of each PCLK pulse occurs at the center of the decoder half-cell "windows" i.e., midway between the times at which potential flux transitions occur. One-shot A14-5 is adjustable allowing PCLK to be moved with respect to the decoding window. This provides a means of optimizing the window adjustment and of measuring the read performance of the drive in terms of error-free range of adjustment. The delay should be set to 1.0 us for normal operation.

Read Data Decoder (See sheet 4 of the schematic)

The decoder consists of flip-flops A13-5, A13-3, A12-3, AND/OR inverter A11-8. Using the inputs RDOS and PCLK from the PLL, this circuit decodes the read data and generates a high output for half a cell-time on RDATA for each flux transition read from the disk. Timing for the read data decode circuit is shown in figure 1-12.

The falling edge of each RDOS pulse toggles A13-5 as shown in figure 1-12. This output is a replica of the flux pattern as it is recorded on the disk. PCLK on A13-12 now samples the output from A13-5 at the center of each half-cell window causing A13-3 to set or reset accordingly. A13-3 is then delayed one half-cell by A12-3. AND/OR inverter A11-8 is connected as exclusive OR and detects any change of state at A13-3. The output, RDATA, goes high for half a cell-time when any flux transition (data or clock) is detected.

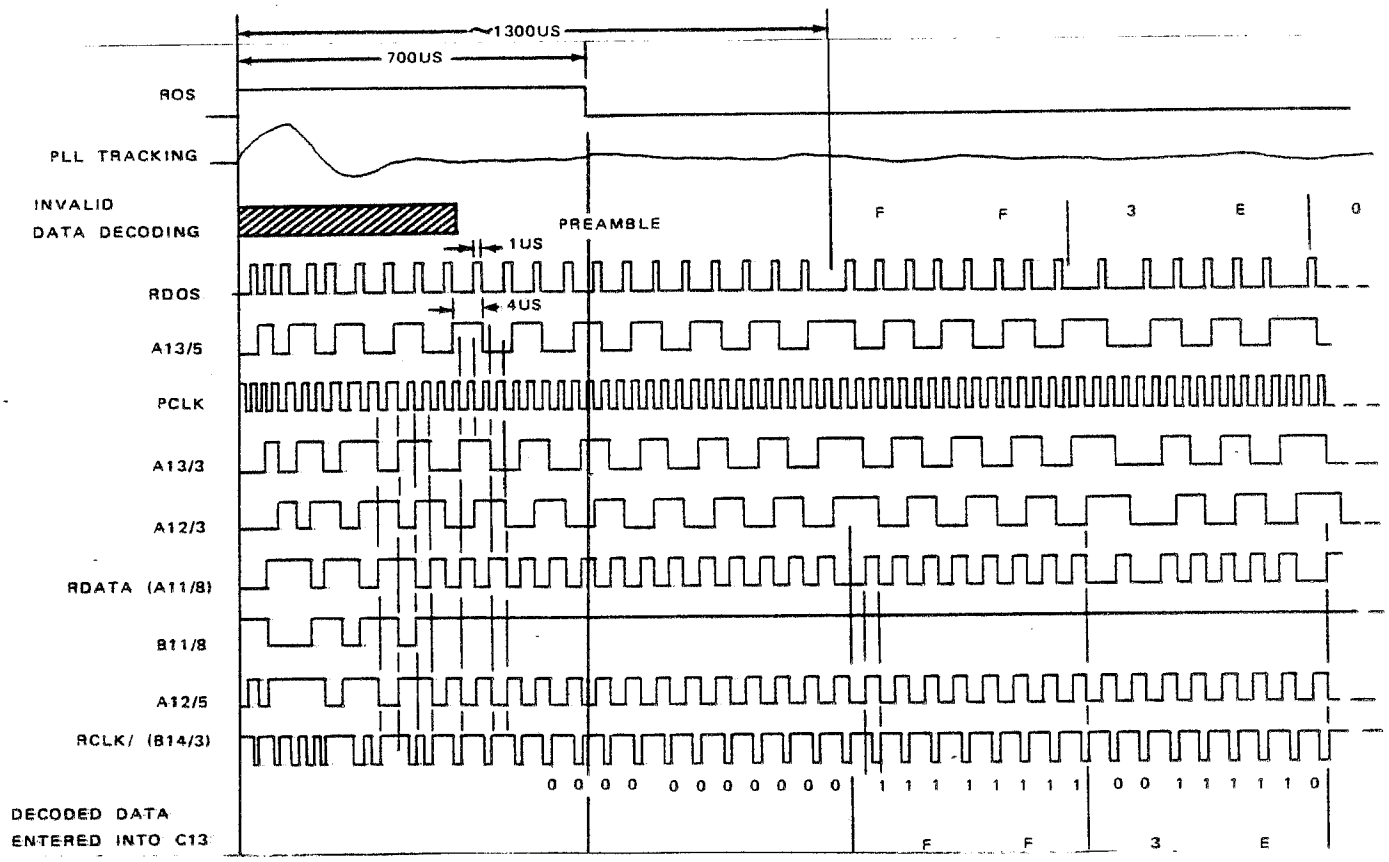


Figure 1-12. Read Decoding and Sync Circuits, Timing Diagram

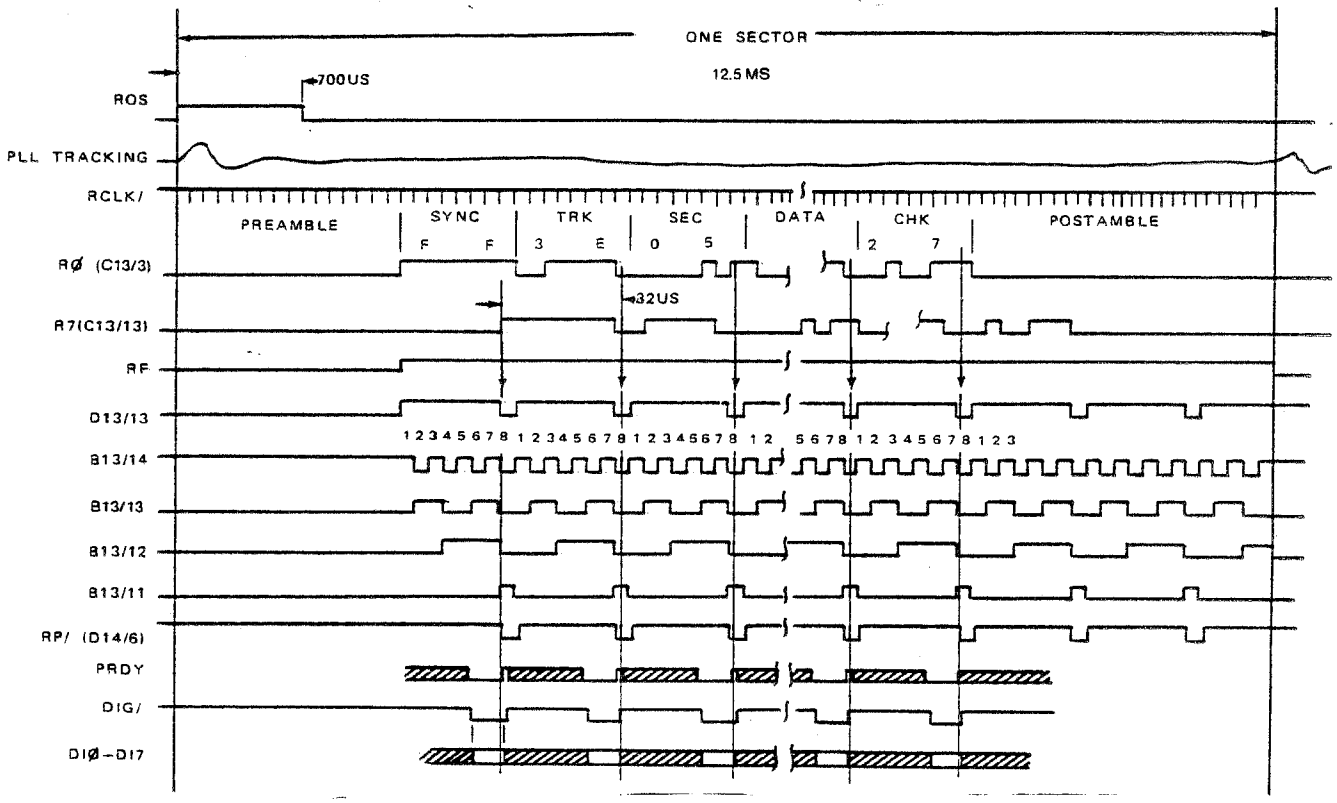


Figure 1-13. Read Logic, Timing Diagram

Read Clock Synchronization (See sheet 4 of the schematic)

The circuit consisting of B11-8, A12-5, and B14-3 generates a clock signal, RCLK, for the data transitions only which is used to sample the decoding read data. This circuit must be initially synchronized during the preamble so that the correct (data) half-cell is selected.

Flip-flop A12-5 is clocked by PCLK causing the output to change state for each half-cell that NAND output B11-8 is high. A clock pulse is generated on RCLK/ when A12-5 is high as shown in figure 1-12. In the preamble area that data pattern is known to be all zeroes; i.e., no transitions should be detected in the data half-cell. During the first 700 us of preamble (ROS high), B11-8 tests for this condition and the output goes low for one half-cell if a one-bit is detected. This inhibits A12-5 from changing state one time causing the other half-cell to be selected. Note the period of ROS is long enough to cover both sector-hole tolerancing and the PLL lockup time. During the remainder of the sector B11-8 remains high and RCLK/ pulses are generated during every half-cell.

Read Shift register and Control Logic (See sheet 4 of the schematic)

Shift register C13 assembles the decoded data into byte-parallel form for transmission to the CPU. The control logic consisting of B12-9, D13-3, B13, and D14-6 generates two control signals, RF and RP/, which coordinate the transfer of each byte. See figures 1-12 and 1-13.

C13 and B12-9 are initially held reset during the beginning of each sector by ROS/ low. When ROS/ goes high, zero bits are entered into the register until the first bit of the sync byte is encountered. At this time, C13-3 goes high and the rising edge clocks B12-9, causing RF to set. RF true causes TF (transfer flag) to go true, signifying the the first (sync) byte is almost ready to transfer.

Counter B13 is intially preset to a count of one by a low output on D13-13. When RF goes true, the preset condition is removed and the counter counts off consecutive groups of eight bits corresponding to each byte. A fully assembled byte is available in the shift register when a count of eight is reached. At this time, the high output at B13-11 is delayed by 200 us, then inverted to form RP/. RP/ low forces PRDY high allowing the CPU to complete execution of the current instruction (read from read data register). B13-11 high also produces a low on D13-13, causing the counter to be preset to one again at the beginning of the following byte. The remaining bytes of the sector are transferred in this manner.

1.1.8 Data In Bus Multiplexing (See sheet 5 of the schematic)

This logic gates PROM, status, or read data information onto the S-100 data-in bus according to the address specified in the current instruction.

The PROMs C9 and C10 contain a bootstrap program which loads the system software from disk into memory after power-on. The bootstrap is entered by transferring control to the controller base address (normally F800H). A description and listing of this program is given in paragraph 6.7 of the Micropolis User's Manual.

Signals comprising status bytes 0 and 1 and the read register outputs R0 thru R7 are multiplexed together by C4, C5, C11, and C12. Status byte 0 is selected if A1.A0 = 00; status byte 1 if A1.A0 = 01; and the read register is selected if A1 = 1. The tri-state outputs from either the PROMs or C11, C12 are enabled by CSEL or CSEL/ depending on whether the lower or upper half of the 1K controller address space is being accessed. The selected byte is gated onto data-in lines D10 thru D17, by D11 and D12 when DIG/ is low.

II. TESTS AND ADJUSTMENTS

2.1 Controller Adjustments

Controller adjustments consist of:

a. Center frequency adjust.

b. 2 us single-shot adjust.

c. 1 us single-shot adjust.

2.1.1 Test Configuration

a. Insert the controller in an S-100 bus 8080/Z80 based computer using an extender card.

b. Connect controller to any Micropolis storage module.

2.1.2 Center Frequency Adjust Test Procedure

a. Ensure that the drive is not on.

b. Connect oscilloscope to the oscillator output at A15-7. Set oscilloscope time base to 200 ns/cm.

c. Measure frequency of oscillator.

2.1.3 2 us Single-Shot Adjust Test Procedure

a. Insert a diskette in drive.

b. Position the head to track 0 and write a full track of 'ones' data (16 sectors).

c. Perform a continuous read operation on track zero.

d. Alternately select program X14 to achieve steps b and c.

e. Connect oscilloscope to A14-5, set time base of oscilloscope to 200 ns/cm, and observe one-shot output.

2.1.4 1 us Single-Shot Adjust Test Procedure

a. Proceed with steps a thru d, para. 2.1.3.

b. Connect oscilloscope to A14-3, set time base of oscilloscope to 200 ns/cm, and observe one-shot output.

2.1.5 Acceptable Limits

a. Center frequency: 970 kHz minimum - 1033 kHz maximum.

b. 2 us single-shot: 1.94 us minimum - 2.06 us maximum.

c. 1 us single-shot: 0.97 us minimum - 1.03 us maximum.

2.1.6 Adjustment Procedure

a. Center frequency: Adjust R40 until the output frequency is 1 MHz.

b. 2 us single-shot: Adjust R27 for a period of 2 us.

c. 1 us single-shot: Adjust R46 for a period of 1 us.

III. Troubleshooting

3.1 Visual Inspection

Visually inspect the disk controller board as follows:

a. Check for evidence of burnt or damaged components.

b. Check for proper orientation of polarized capacitors.

c. Ensure proper orientation of all jumper selected options (See User's Information Sheet for details).

3.2 Voltage Measurement

Connect the controller to a test system and apply power. Measure the supply voltages as follows:

a. +5 volts at pin 3 of VR-1. +5 volts $\pm$ 5%.

b. -5 volts at pin 4 of B-15. -5 volts $\pm$ 5%.

c. +5 volts filtered at pin 7 of B-15. +5 volts $\pm$ 5% with less than 10 millivolts of ripple.

Should any of these voltages be out of tolerance, refer to the following schematic drawings for location.

a. +5 volts, page 8 of schematic.

b. -5 volts, page 9 of schematic.

c. +5 volts filtered, page 8 of schematic.

3.3 Checksum of Bootstrap PROM's

A checksum of the Bootstrap PROM's can be accomplished by using the system monitor's Q command followed by F800 F8FF for standard systems. Refer to User's Information Sheet at the beginning of this manual for further information on the board's base address.

The checksum of the Bootstrap PROM's is BCH. Should a number other than BC result, check the circuitry on pages 2 or 5 of the schematic.

3.4 Read Operation

To perform a read operation, insert an MDOS diskette with "DIAG" and attempt to boot up. If the diskette does not boot, perform the following check:

a. Check for proper drive selection by checking pin 3 of B-5. Refer to sheet 8 of the schematic. Check all signals on the schematic that relate to the read operation.

b. Check for an indication of RDA at pin 10 of B-7. Refer to sheet 8 of the schematic.

c. Check for the presense of SECP (Sector pulse) at pin 4 of B-7. Refer to page 8 of the schematic.

d. Check for the proper binary counting of S0, S1, S2, and S3 at the appropriate pins of C-3. Refer to page 6 of the schematic.

e. Check for proper pulse widths from the monostable multivibrators C-1, C-2, and D-1. Refer to sheet 6 of the schematic.

f. Check for the presence of PCLK at pin 3 of B-14. Refer to sheet 9 of the schematic.

g. Check for the presence of RDATA at pin 8 of A-11. Refer to sheet 4 of the schematic.

h. Check for the presence of RCLK at pin 3 of B-14. Refer to sheet 4 of the the schematic.

i. Check for the proper operation of "data and status" multiplexers C4, C5, C11, and C12. Refer to sheet 5 of the schematic.

j. Check for the presense of DIG at pin 8 of C-8. Refer to sheet 6 of the schematic.

k. Ensure proper operation of the output data buffers D11 and D12. Refer to sheet 5 of the.

3.5 Write Operation

To perform a write operation, insert an MDOS diskette with DIAG in the proper drive and boot up. Call up DIAG to the monitor and you will see

```
MFM DIAGNOSTIC VS 4.0
800031 REV A
```

on the screen.

Respond to DIAG as follows:

```
FRONT PANEL (Y OR N)?N
ENTER HIGH TRACK 76
ENTER COMMAND Z,0,0,I,2
```

The above command will initialize the drive to track 0 and write a binary progression on all sectors of all tracks.

```
ENTER COMMAND RD,2
```

This command will attempt to read the pattern written by the command I,2. Any errors will be displayed on the screen. See Micropolis Manual, Section 8.3.5, Page 8.2 for error message explanations.

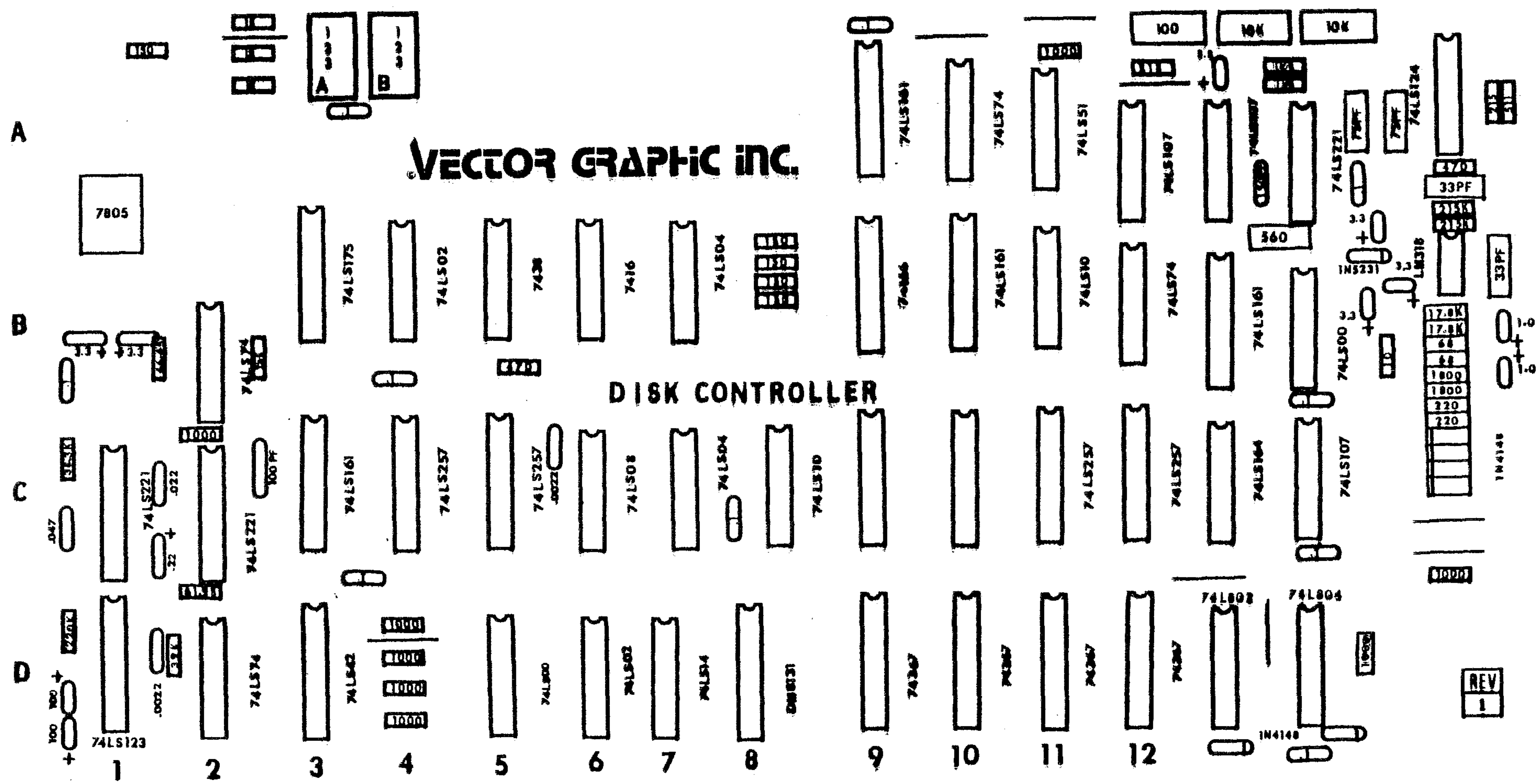
Should errors occur at this point, the problem is not a read error, the problem is in the write circuit. Check the following if this problem should occur.

a. Check for WRT at B6 pin 8. Refer to page 8 of the schematic.

b. Check for WDA at B6 pin 10. Refer to page 8 of the schematic. If this signal is present, it may be incorrect due to a malfunction in the parallel to serial converter B9, shown on sheet 3 of the schematic. Although a signal is present at WDA a serial to parallel converter will reveal an incorrect output.

c. If WDA is not present, check the clock signal at A10 pin 11 and the circuitry on sheet 3 of the schematic.

d. Should all of the above signals be absent, check the circuitry on sheet 2 of the schematic.



VECTOR GRAPHIC inc.
DISK CONTROLLER
A
B
C
D
1
2
3
4
5
6
7
8
9
10
11
12
7805
74LS123
74LS221
74LS74
74LS175
74LS02
7438
7416
74LS04
74LS161
74LS257
74LS08
74LS10
74LS00
74LS14
DM8131
74367
74LS74
74LS51
74LS107
74LS164
74LS124
LM318
1N5231
1N4148
74LS02
74LS04
100
10K
33PF
75PF
360
100 PF
REV
1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	RELEASE	4/5/77	
	B	EN00058 CHANGE HSLT PINOUT	1/10/78	
	B1	EN00109	4/25/78	
	C	EN0121	6/6/78	

[5] TABLE I

PART NO.	REF. DESIGNATION
100-0100-6	R47
-0680-7	R32,35
-1500-6	R18,19,20,21,22
-2200-2	R28,29
-4700-3	R43,42
-1202-9	R26,45
-1001-5	R1,2,3,4,6,7,14, 15,23,24,25,48
-1801-8	R30,31
-1502-2	R8
-3902-2	R12
-2203-6	R17
-3301-7	R16
-0000-8	R5,41
101-5600-8	R39
105-2150-8	R36,43
-5110-9	R44
-1782-9	R34,38
-3832-0	R11
-4642-2	R10
-6192-6	R9
-2153-2	R37,78
130-1002-0	R27,46
-1000-4	R40
160-0330-3	C11,20,21
-0750-2	C19
-1000-1	C2
-1500-0	C16
-7500-4	C[illegible]
161-2201-3	C6,7
-2202-0	C4
162-4702-5	C5
163-2203-4	C3
-1004-7	C17,18
-3304-9	C13,14,22,23,26,27

[4] TABLE I (CONT.)

PART NO.	REF. DESIGNATION
165-1002-6	C12,15,28 THRU 36
173-1006-1	C9,10
200-4446-7	CR1 THRU 6
210-5231-1	CR7
380-7805-1	VR1
400-0000-2	B14,D5
-0002-0	B4,D1,L13
-0004-4	B7,C7,D14
-0008-5	C6
-0010-1	B11,C8
-0014-3	D7
-0042-4	C3
-0051-5	A11
-0074-7	A10,B2,B12,D2
-0107-5	A12,A13,C14
-0123-2	D1
-0124-0	A15
-0161-2	A9,B10,B13,C3
-0164-6	C13
-0175-2	B3
-0221-4	A14,C1-C2
-0257-8	C4,C5,C11,C12
401-0016-6	B6
-0038-0	B5
-0166-9	B9
-0367-3	D9,D10,D11,D12
408-0003-9	D8
410-0318-7	B15
65[illegible]-8	HEATSINK
[illegible]-1603-9	SOCKET C9,C10
-0503-2	CONNECTOR J3
684-0003-5	FP1,2,3

[6] TABLE II

ASSY. 100086 DASH NO	VERSION CHARACTERISTIC	JUMPERS (PART NO. 100-0000-8) W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15	W16	XTAL1	C24 C1	C25	PROM C10	PROM C9
01-6	ADDRESS F4 MFM EXT OSC.			X			X	X					X		X		X			100 PF 160-1000-1	800001-01-8	800001-02-6
02-4	ADDRESS F4 MFM INT OSC.			X			X	X				X			X		X	2.0 MHZ 500-2004-9		100 PF 160-1000-1	800001-01-8	800001-02-6
03-2	ADDRESS F4 DF EXT OSC.			X		X			X				X	X		X				150 PF 160-1500-0	800001-01-8	800001-02-6
-04-0	ADDRESS F4 DF INT OSC.			X		X			X			X		X		X		2.0 MHZ 500-2004-9		150 PF 160-1500-0	800001-01-8	800001-02-6
-52-9	ADDRESS F4 MFM, INT OSC, RELOC. PROMS			x			x	x				x			x		x	2.0 MHZ 500-2004-9		100 PF 160-1000-1	800003-01-4	800003-02-2

[7] TABLE III

LAST USED	DELETED
R48	
C36	
CR7	
VR1	
XTAL 1	
TP3	
J3	
W16	
U47	

[7] FOR LAST USED AND DELETED REF DESIGNATION SEE TABLE III.

[6] FOR COMPONENTS AFFECTED BY VERSION SEE TABLE II.

[5] FOR PART NO OF COMPONENTS NOT AFFECTED BY VERSION SEE TABLE I.

4. FOR PCBA SEE DRAWING NO. 100086.

3. ALL DIODES ARE 1N4446.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS.

1. ALL RESISTOR VALUES ARE IN OHMS. 1/4W, ±5%.

NOTE: UNLESS OTHERWISE SPECIFIED:

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

DR BY

CHK BY

APPROVED BY

NEXT ASSY | USED ON

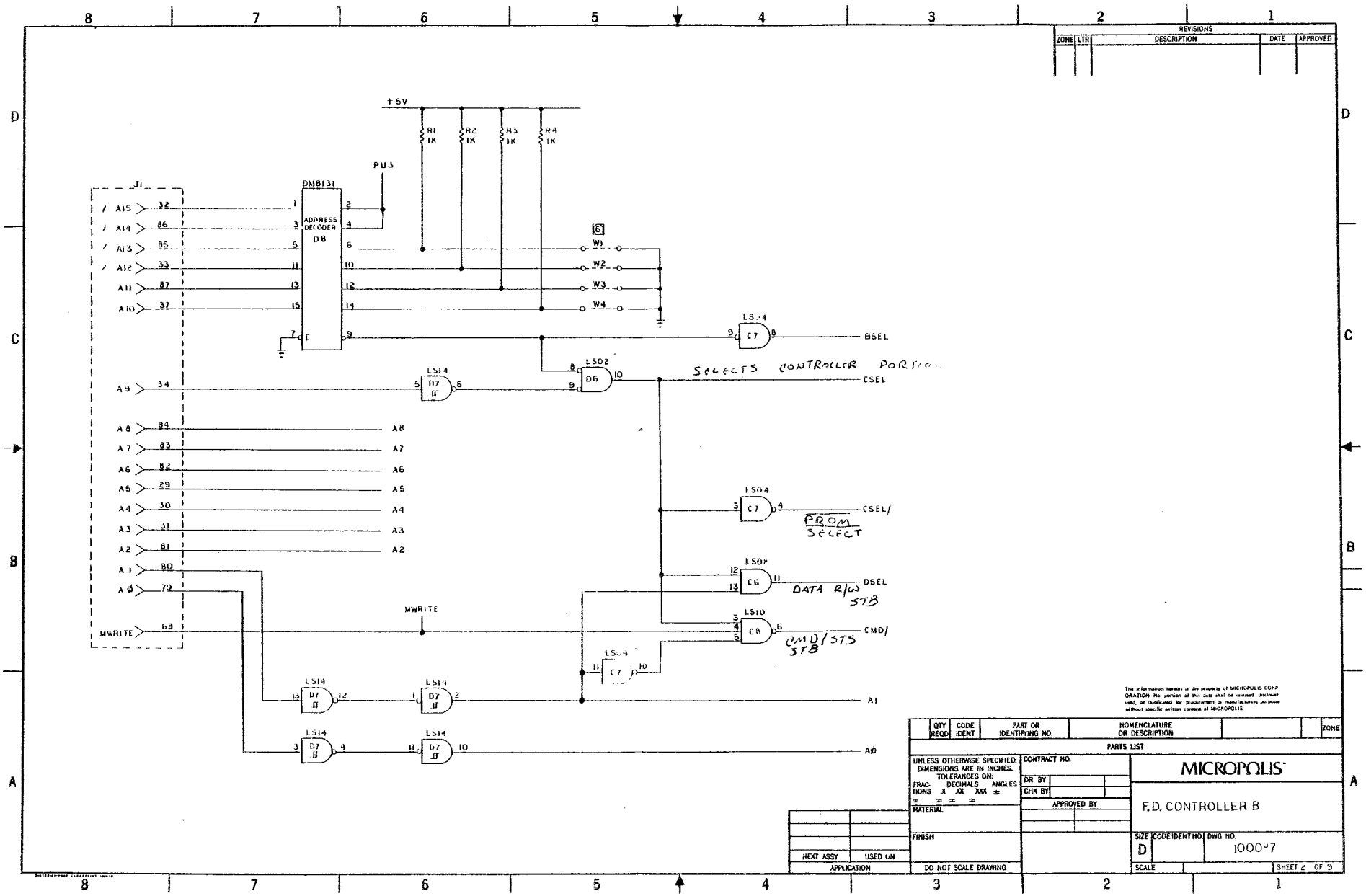
APPLICATION

MICROPOLIS

F.D. CONTROLLER B

SIZE	CODE IDENT NO	DWG NO.	REV
D		100087	C

SCALE | SHEET 1 OF 9



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION		ZONE
PARTS LIST					

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ± .X ± .XX ± .XXX ± ANGLES ±

MATERIAL

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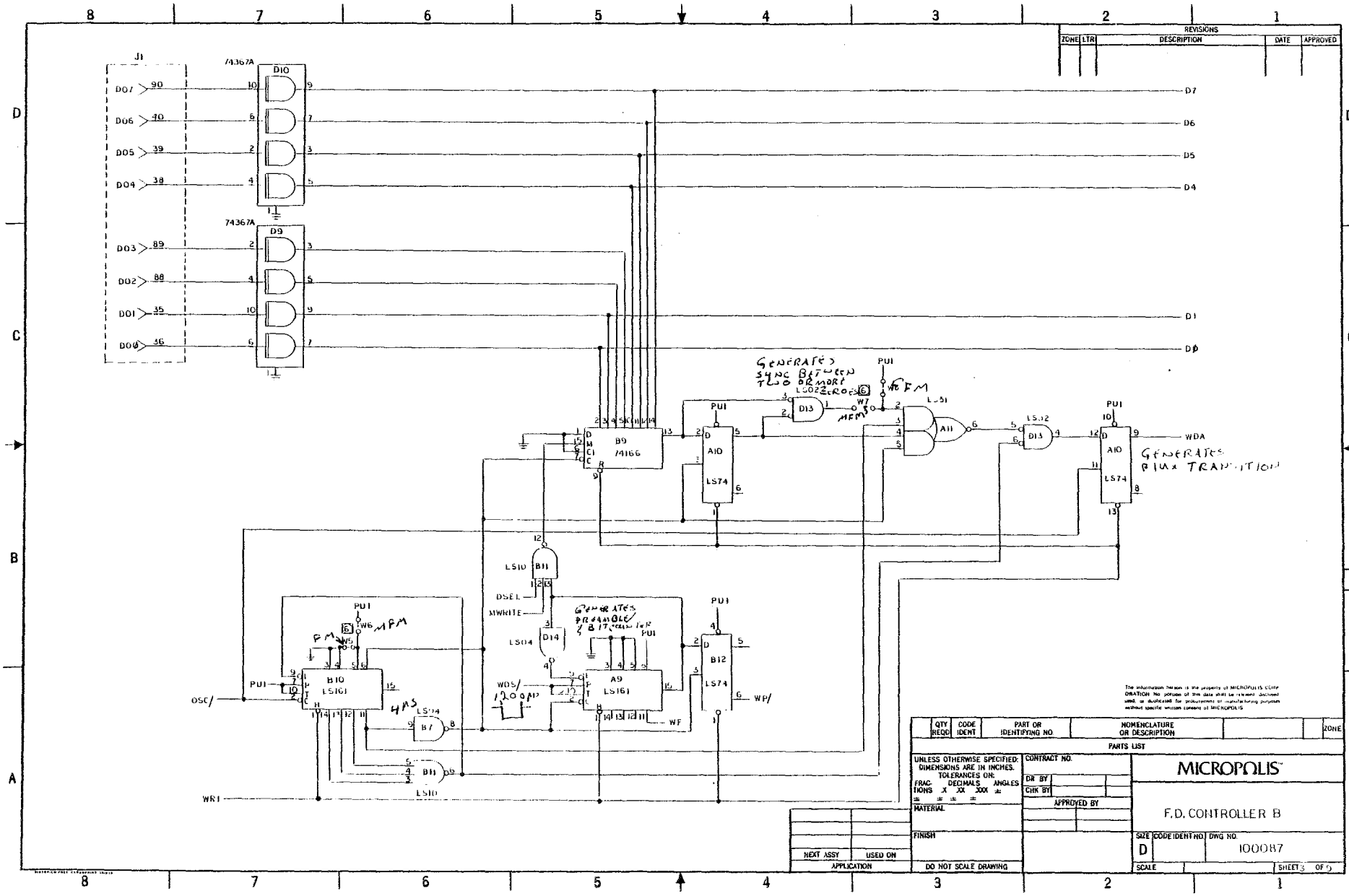
MICROPOLIS

F.D. CONTROLLER B

SIZE	CODE IDENT NO	DWG NO.
D		100097

SCALE | SHEET 2 OF 5


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
J1
74367A
D10
D9
DO7
DO6
DO5
DO4
DO3
DO2
DO1
DO0
D7
D6
D5
D4
D1
D0
GENERATES SYNC BETWEEN TLS0 & MFM
LS02 ZEROES
WE FM
WE MFM
PU1
B9 74166
A10 LS74
D13
A11 LS51
LS32
A10 LS74
WDA
GENERATES RMX TRANSITION
LS10 B11
DSEL
MWRITE
LS04 D14
GENERATES PREAMBLE & BIT CELLS FOR MFM
WDS/
A9 LS161
B12 LS74
WF
WP/
B10 LS161
FM
MFM
OSC/
4MS
LS04 B7
LS10 B11
WR1
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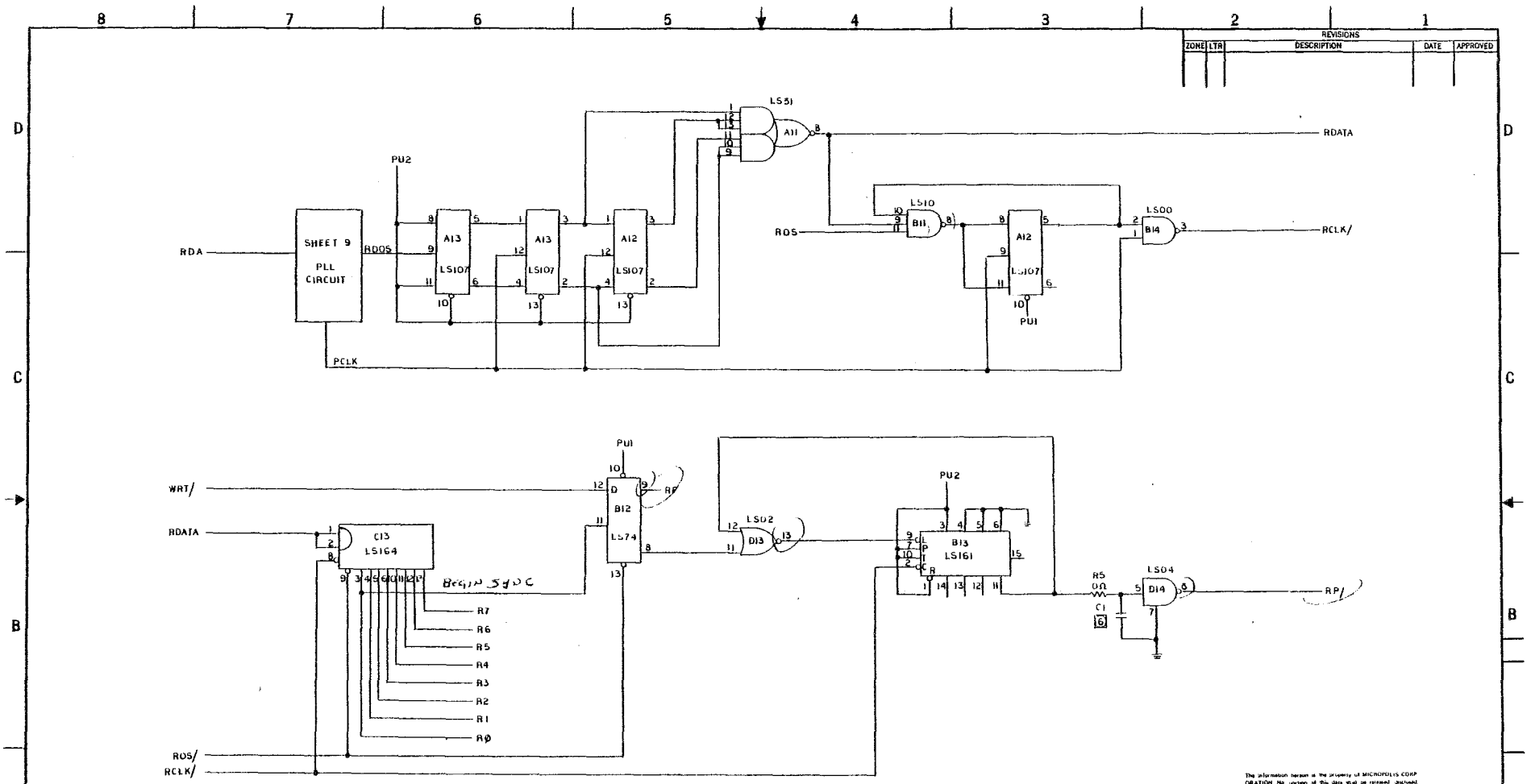
MICROPOLIS
F.D. CONTROLLER B
SIZE D | CODE IDENT NO. | DWG NO. 100087
SCALE | SHEET 3 OF 9


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
RDA
SHEET 9
PLL
CIRCUIT
RDOS
PCLK
PU2
A13
LS107
A12
LS51
A11
RDATA
LS10
B11
RDS
LS00
B14
RCLK/
PU1
WRT/
RDATA
C13
LS164
B12
LS74
RP
LS02
D13
B13
LS161
R5
0Ω
C1
16
LS04
D14
RP/
R7
R6
R5
R4
R3
R2
R1
R0
RDS/
RCLK/
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
ZONE
PARTS LIST
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS DECIMALS ANGLES .X .XX .XXX
CONTRACT NO.
DR BY
CHK BY
APPROVED BY
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
MICROPOLIS
F.D. CONTROLLER B
SIZE
CODE IDENT NO
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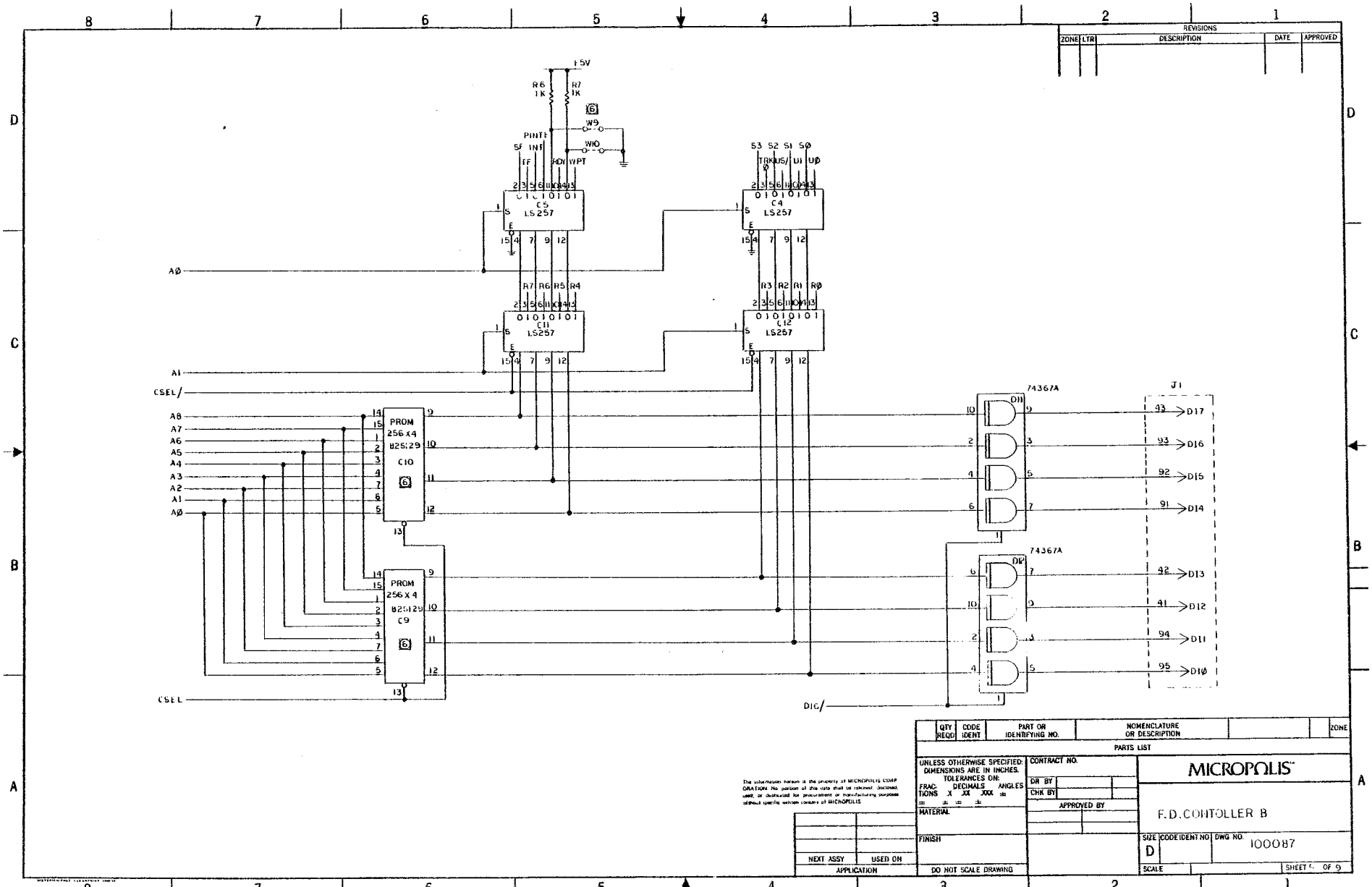
100087
SCALE
SHEET 4 OF 9


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
+5V
R6 1K
R7 1K
W9
W10
PINTE
SF INF
FF
RDY WPT
S3 S2 S1 S0
TRK0/ U1 U0
C5 LS257
C4 LS257
C11 LS257
C12 LS257
A0
A1
CSEL/
CSEL
A8
A7
A6
A5
A4
A3
A2
A1
A0
PROM 256x4 82S129 C10
PROM 256x4 82S129 C9
74367A D11
74367A D12
J1
D17
D16
D15
D14
D13
D12
D11
D10
DIG/
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
ZONE
PARTS LIST
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS X .XX .XXX DECIMALS ANGLES
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APPLICATION
MICROPOLIS
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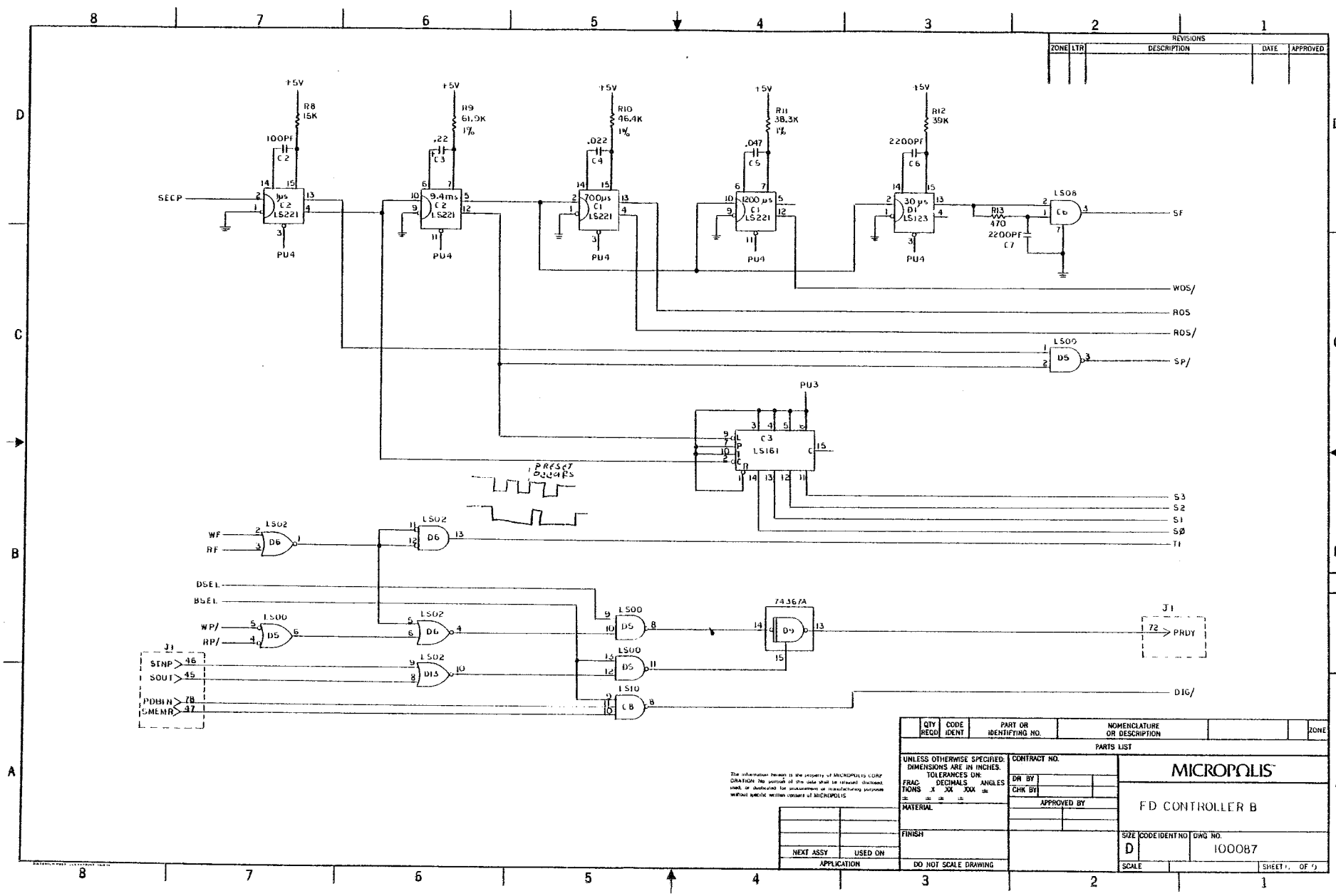
SIZE D
CODE IDENT NO
DWG NO. 100087
SCALE
SHEET 6 OF 9


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
+5V
R8 15K
100PF C2
SECP
9µs C2 LS221
PU4
R9 61.9K 1%
.22 C3
9.4ms C2 LS221
R10 46.4K 1%
.022 C4
700µs C1 LS221
R11 38.3K 1%
.047 C5
1200µs C1 LS221
R12 39K
2200PF C6
30µs D1 LS123
R13 470
2200PF C7
LS08 D6
SF
WOS/
ROS
ROS/
LS00 D5
SP/
PU3
C3 LS161
PRESET 0.04µS
S3
S2
S1
SØ
T1
LS02 D6
WF
RF
DSEL
BSEL
LS00 D5
WP/
RP/
LS02 D6
LS02 D13
J1
SINP 46
SOUT 45
PDBIN 78
SMEMR 97
LS00 D5
LS00 D5
LS10 C8
7436/A D9
J1
72 PRDY
DIG/
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | ZONE
PARTS LIST
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS .X .XX .XXX ANGLES
MATERIAL
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NEXT ASSY USED ON
APPLICATION
DO NOT SCALE DRAWING
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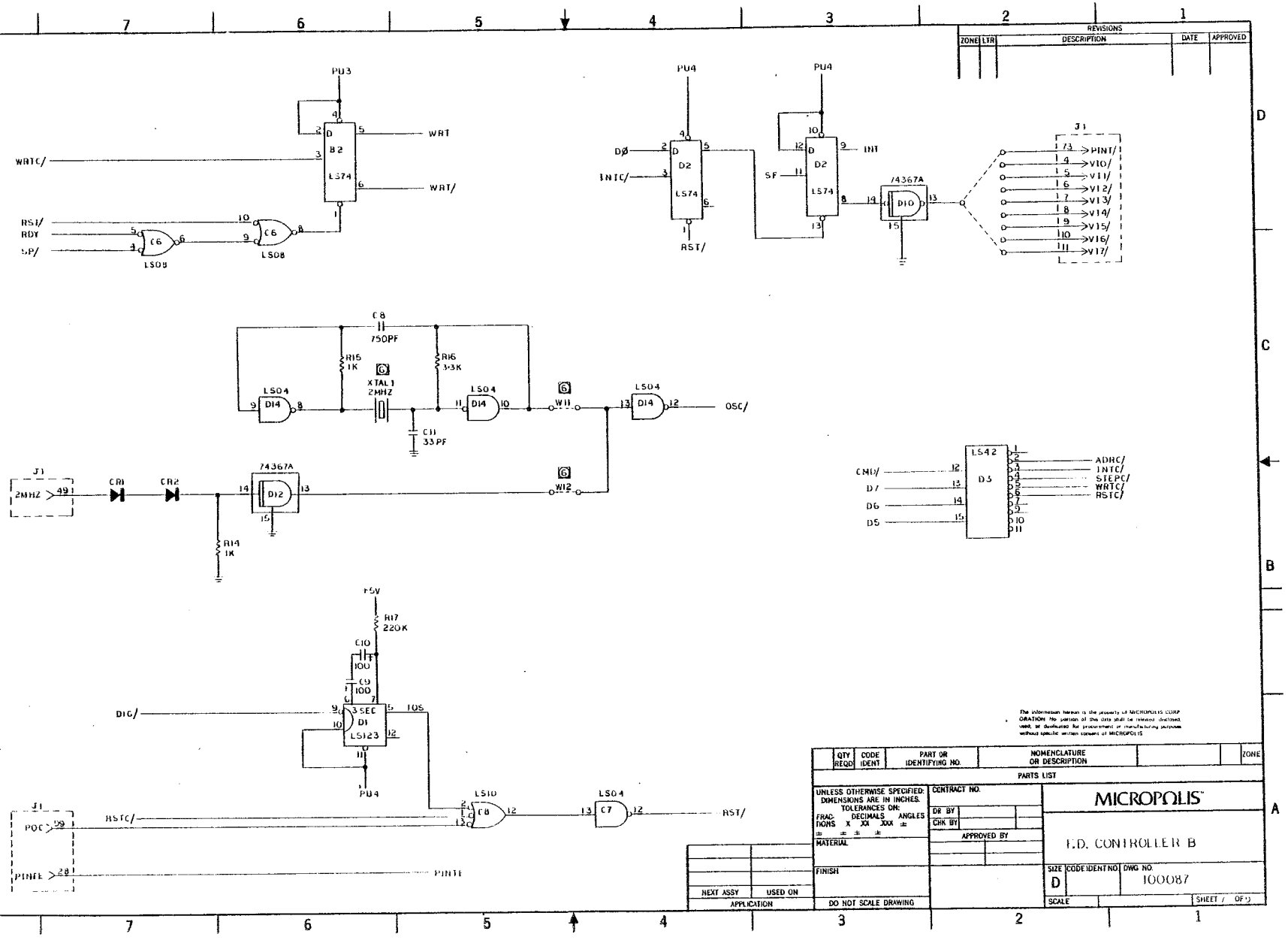
MICROPOLIS
FD CONTROLLER B
SIZE D CODE IDENT NO DWG NO. 100087
SCALE SHEET 1 OF 9


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
PU3
WRTC/
B2
LS74
WAT
WAT/
RST/
RDY
SP/
C6
LS08
PU4
DØ
INTC/
D2
LS74
INT
SF
RST/
74367A
D10
J1
PINT/
V10/
V11/
V12/
V13/
V14/
V15/
V16/
V17/
C8
750PF
R15
1K
R16
3.3K
XTAL1
2MHZ
C11
33PF
LS04
D14
W11
OSC/
J1
2MHZ
CR1
CR2
74367A
D12
W12
R14
1K
LS42
D3
CMD/
D7
D6
D5
ADRC/
INTC/
STEPC/
WRTC/
RSTC/
+5V
R17
220K
C10
100
C9
100
DIG/
3 SEC
D1
LS123
105
PU4
LS10
C8
LS04
C7
RSTC/
RST/
J1
POC
PINTE
PINTE
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SIZE D
CODE IDENT NO
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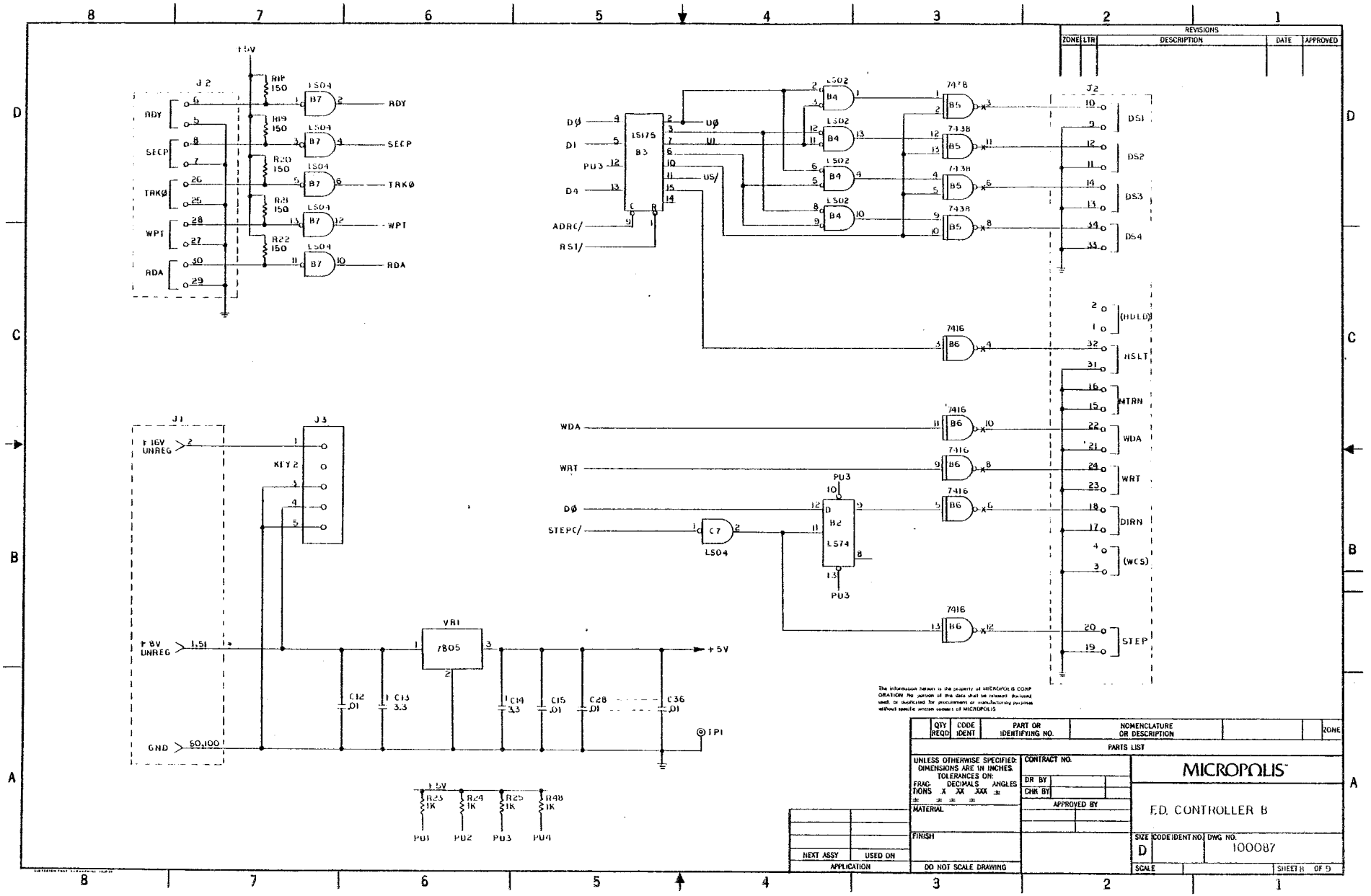
REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
J2
RDY
SEEP
TRKØ
WPT
RDA
R18 150
R19 150
R20 150
R21 150
R22 150
LS04
B7
RDY
SEEP
TRKØ
WPT
RDA
DØ
DI
PU3
D4
ADRC/
RS1/
LS175
B3
UØ
UI
US/
LS02
B4
7438
B5
DS1
DS2
DS3
DS4
7416
B6
(HDLD)
HSLT
HTRN
WDA
WRT
DIRN
(WCS)
STEP
WRT
DØ
STEPC/
C7
LS04
PU3
B2
LS74
J1
+16V UNREG
+8V UNREG
GND
50,100
J3
KEY 2
VR1
7805
+5V
C12 .01
C13 3.3
C14 3.3
C15 .01
C28 .01
C36 .01
TP1
+5V
R23 1K
R24 1K
R25 1K
R48 1K
PU1
PU2
PU3
PU4
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PARTS LIST
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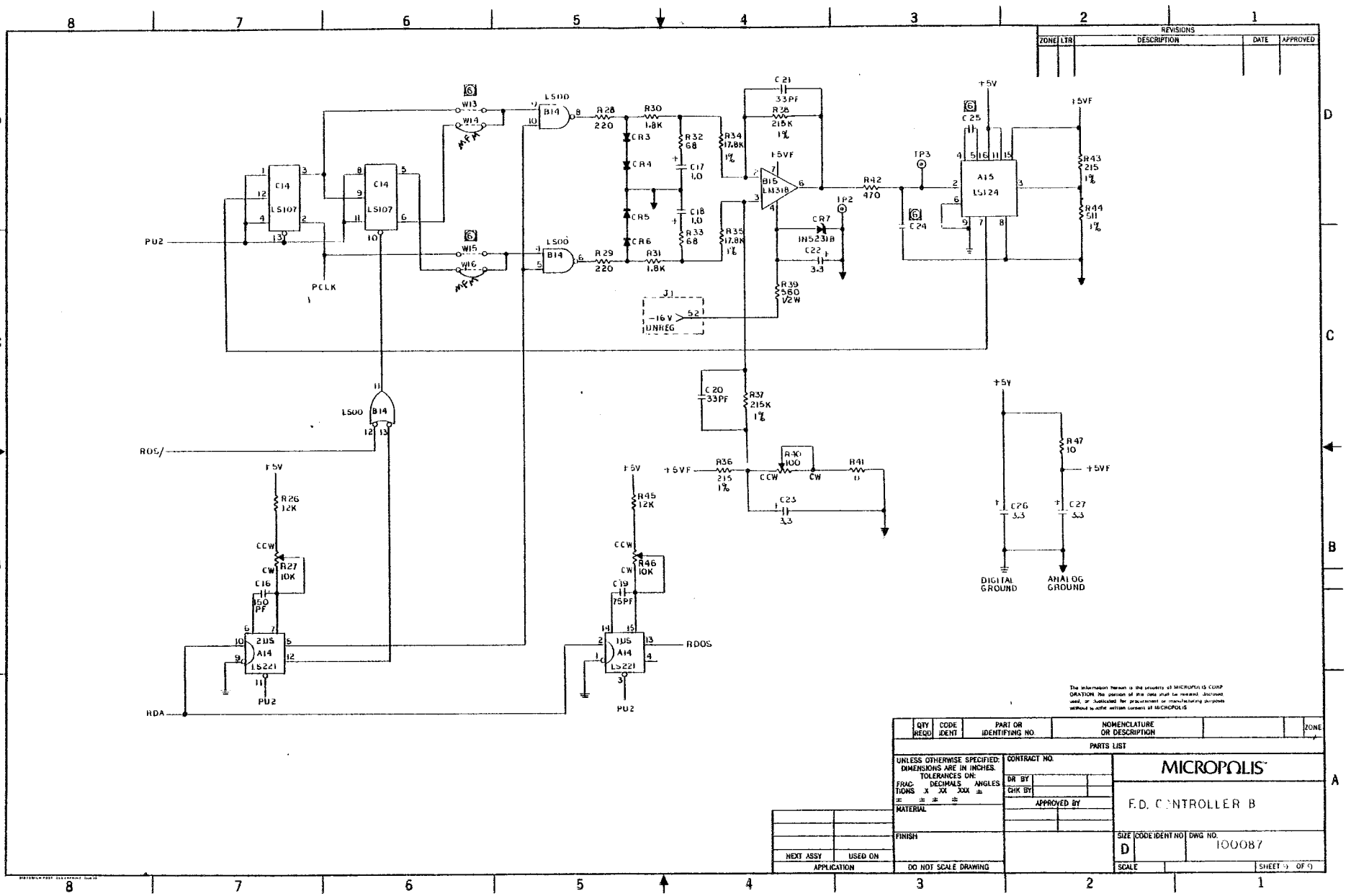
MICROPOLIS
F.D. CONTROLLER B
SIZE D
CODE IDENT NO.
DWG NO. 100087
SCALE
SHEET 8 OF 9
NEXT ASSY
USED ON
APPLICATION


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
+5V
+5VF
PU2
PCLK
RDS/
RDA
RDOS
-16V UNREG
DIGITAL GROUND
ANALOG GROUND
MFM
MFM
CCW
CW
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APPLICATION
DO NOT SCALE DRAWING
MICROPOLIS
F.D. CONTROLLER B
SIZE
CODE IDENT NO
DWG NO.
100087
SCALE
SHEET 9 OF 9

MICROPOLIS RIGID DISK
SUGGESTED POWER SUPPLY SOURCES

MICROCOMPUTER POWER INC.
JIM ARMSTRONG
2272 CALLE DE LUNA
SANTA CLARA, CA 95050
408 - 988-0265
PART NUMBER CP151M124

POWER-ONE INC.
LARRY STEEN
POWER ONE DRIVE
CAMARILLO, CA 93010
805 - 484-2806 213 - 889-4600
PART NUMBER CP379-1

7-30-80